

LCD COLOUR TV

SERVICE MANUAL

CHASSIS NO. : LS01+DVB-T

Please read this manual carefully before service.

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Appendix: 1. Circuit Schematic diagram

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Chapter 1: Specifications and Composition

1. Models for LS01 chassis :

Region	Europe				Asia
Original Models	LT26GJ01EB	LT32GJ01EB	LT37GJ01EB	LT26GJ12EB	LT26GJ01AUB LT32GJ01AUB
	LT32GJ12EB	LT37GJ12EB	LT26GJ88EB	LT32GJ88EB	LT37GJ01AUB LT42GJ01AUB
	LT37GJ88EB	LT26GJ01EBS	LT32GJ01EBS	LT37GJ01EBS	LT32GJ12AUB LT37GJ12AUB
	LT26GJ12EBS	LT32GJ12EBS	LT37GJ12EBS	LT26GJ88EBS	LT26GJ88AUB LT32GJ88AUB
	LT32GJ88EBS	LT37GJ88EBS			LT37GJ88AUB

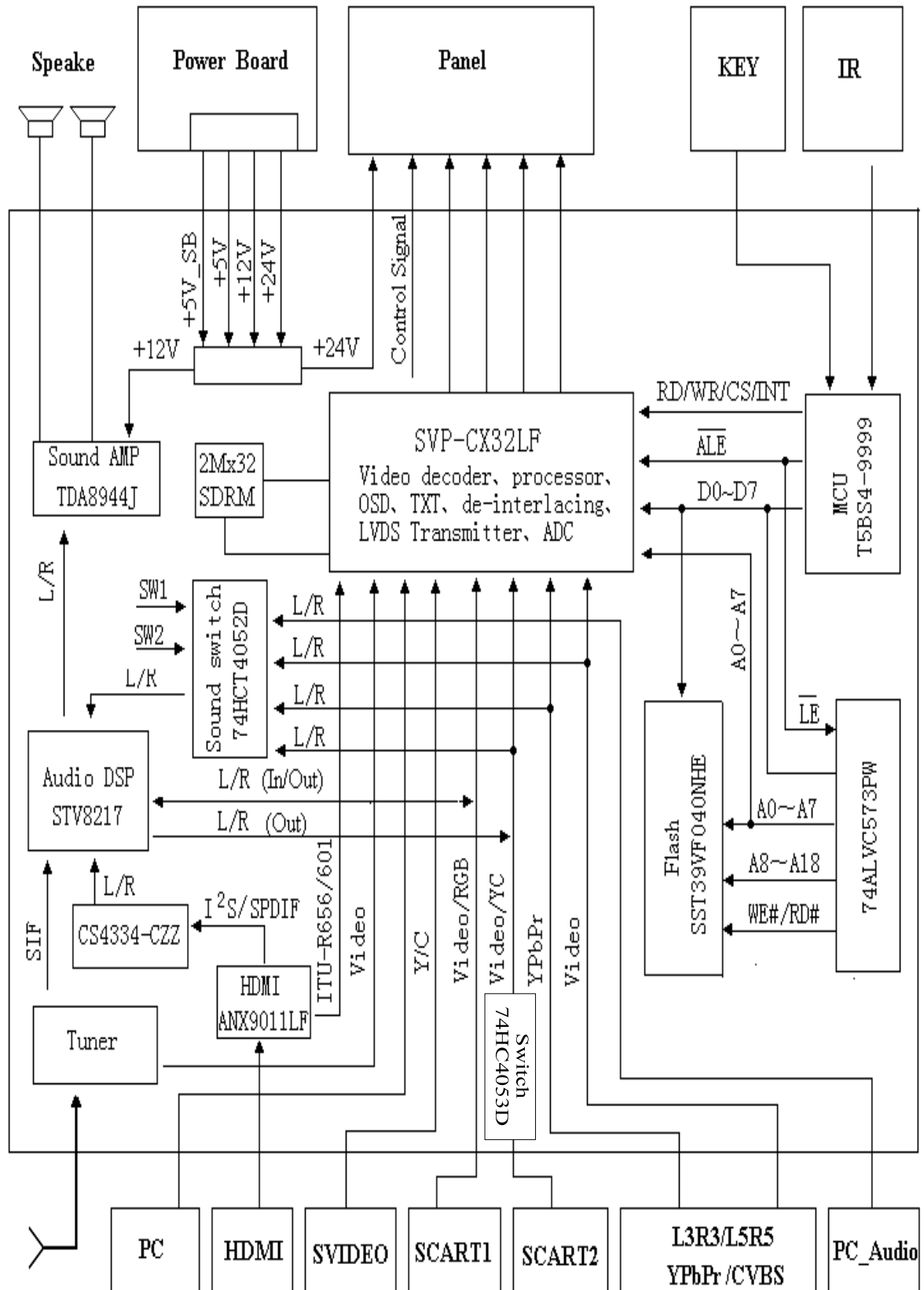
2. Main Feature

Region		Europe	America	Other regions
RF signal	Color system	PAL、SECAM	NTSC、PAL M、PAL N	PAL、NTSC、SECAM
	Sound system	D/K、B/G、I、L/L'	M	D/K、B/G、I、M
Video or Y/C signal		PAL、NTSC、SECAM	PAL、NTSC、SECAM	PAL、NTSC、SECAM
Program presetting		100 (0-99)	68 (AIR: 2-69) 125 CABLE: 1-125)	236 (0-235)
Audio output (THD≤7%)		5W+5W	5W+5W	5W+5W
Power source		100V~240V	100V~240V	100V~240V
Teletext		100 pages	X	100 pages
CCD		X	Yes	X
Sound demodulator		NICAM、IGR	BTSC	NICAM、IGR
SCART		Yes	X	X
VGA		Yes	Yes	Yes
YPbPr		Yes	Yes	Yes
HDMI		Yes	Yes	Yes
Earphone		Yes	Yes	Yes
OSD language		English, French, German, Italian, Portuguese etc.	English, French, Portuguese, Spanish etc.	English, French, German, Spanish etc.
Auto Off without Signal Reception		5 minutes		
Program booking		5 program booking. Turn to the corresponding program at the booking time.		
Swap		Customer could rearrange the channels according to personal habit		
Energy saving system		Customer could adjust LCD screen backlight brightness manually to save energy.		
Plug and Play		LCD TV could be used as computer screen, no need for the installation of software, which is Plug and Play in real sense		

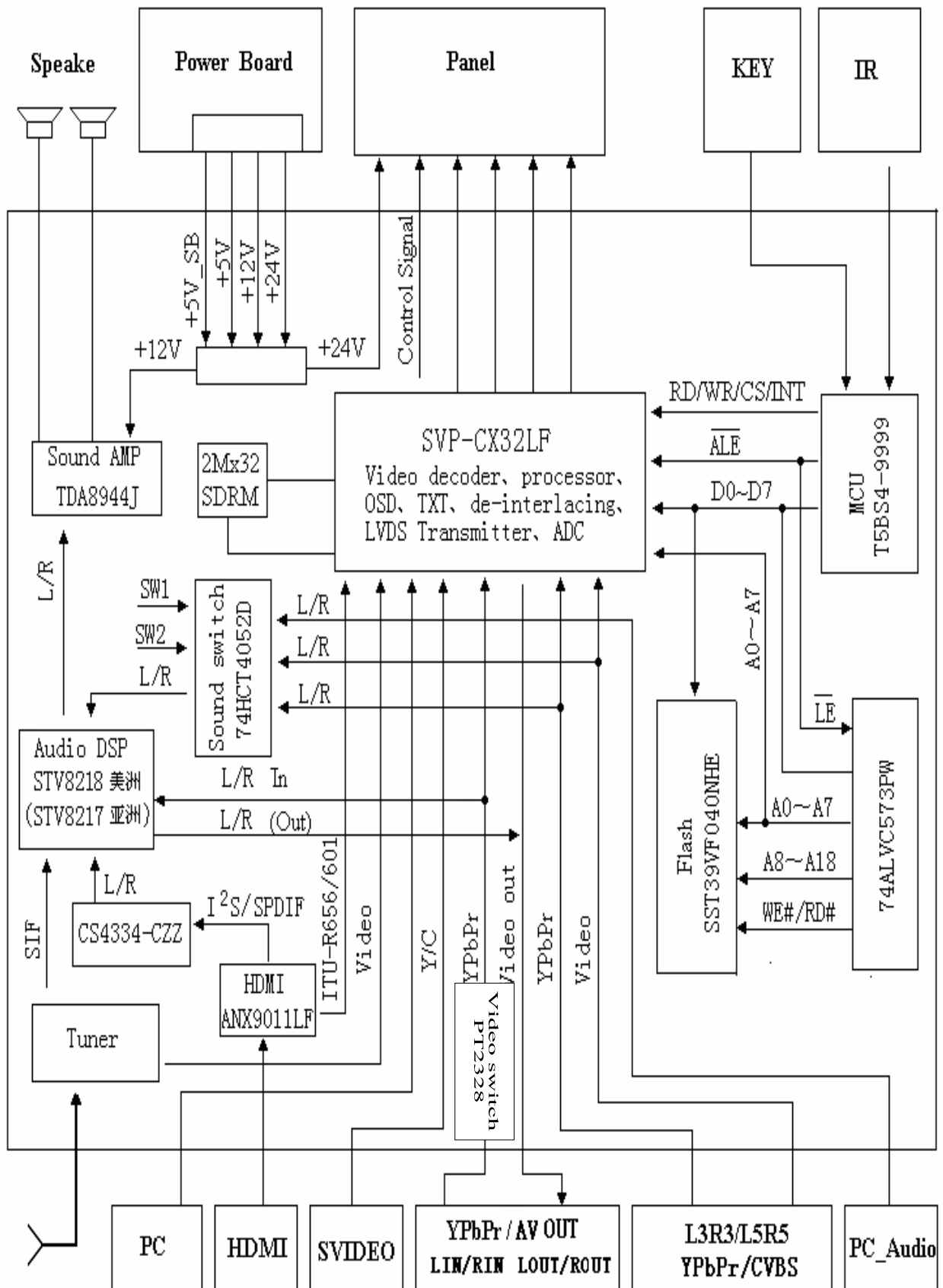
3. Unit IC Compositions:

LCD TV with LS01 chassis is made up of switch power, system control circuit, video processing circuit, audio processing circuit, Power Amplifier circuit, AV input circuit, LCD screen module. Block circuit diagram is shown as below:

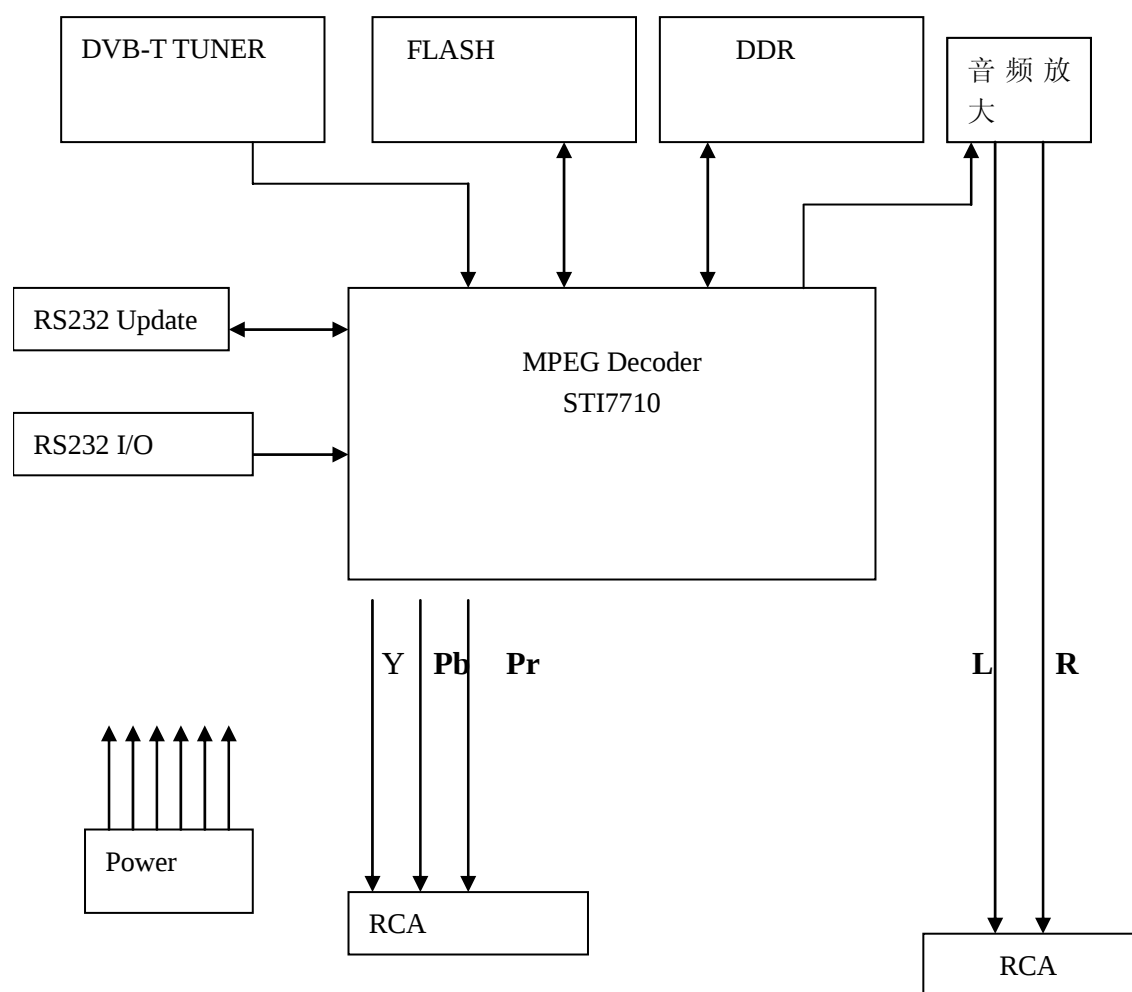
1) European market:



2). American and Asian market:



3) DVB Module



4. Introduction of PCB module

LCD TV with LS01 is made up of power board, side AV board, remote control reception board, key board, and mainboard. The table below is the introduction of the function of all printed board modules.

No.	Parts	Description
1	Mainboard module	Mainboard module is the core of LCD TV signal processing. Under the control of the system control circuit, It undertakes the task of converting the external input signal into the unified digital signal that the LCD screen could identify. Mainboard controls the whole machine through IIC bus, decode VIDEO signal, controls the Video (brightness, contrast, chroma, hue, definition etc), white balance adjusts, generates OSD, de-interlaces signal, converts signal frequency, and finishes signal A/D and D/A conversion, video enhancement, LVDS signal coding and output; it has Scart , S-Video, AV , YPbPr, HDMI and PC interface, Tuner input, sound demodulation, sound processing, sound power amplifier, and online update.

2	Remote reception module	The remote reception board module is constituted by an indicator-light and a remote reception. Customer could manipulate the LCD TV by using remote controller very conveniently. By the color of the indicator light, the operation mode of the LCD TV could be judged (red is standby, green is power on).
3	Built-in power board module	Convert the 100V~240V (50/60HZ) AC into DC, output have +24v, +12V, +5V, and the +5V_STB in standby state.
4	Keyboard module	Keyboard module has 7 function keys (program +/-, volume +/-, AV/TV, menu ,power), customer could use the key to operate the TV freely.
5	LCD screen module	LCD screen has built-in inverter that convert DC into high voltage AC signal to turn on the backlight CCFL (Cold Cathode Fluorescent Light); the LCD screen process the video signal from signal board and reappear.
6	Side AV board	Side AV board is used for earphone output.

Chapter 2: Function Introduction of Main IC

1. Main ICs and functional modules of LS01 chassis

No.	Item no.	Model	Main function
1	J11	JS-6G1/111A25-A2	Tuner output sound IF and video signal
2	U1	SVP-CX32LF	Video decoder, image processor, A/D and D/A conversion
3	U2	IS42S32200C1-6TL	SDRAM with 2MX32bits
4	U3	AT24C64A-10PU-2.7	EEPROM
5	U4	T5BS4-9999	MCU
6	U5	SST39VF040-70-4C-NHE	Flash, Store the Control program.
7	U6	74ALVC573PW	Address latch, to latch the address wires
8	U8	TCM809SENB713	Hardware reset IC of MCU
9	U9	74HCT4052D	Audio input switch of AV terminal
10	U35	STV-8217/STV-8218	Audio signal processor
11	U14	74LVC14AD	VGA line and field synchronizing signal waveform shaping
12	U16、U25	AT24C02BN-10SU-1.8	EEPROM
14	U18、U22	AZ1117H -1.8TRE1	3.3V to 1.8V DC conversion
16	U19、U24	AZ1117H -3.3TRE1	5V to 3.3V DC conversion
18	U20	AZ1084S -3.3TRE1	5V to 3.3V DC conversion
19	U21	AZ1084S -1.8TRE1	5V to 1.8V DC conversion
20	U23	AZ78L08ZTR-E1	12V to 8V DC conversion
21	U26	CS4344-CZZ	HDMI digital audio decode, DAC
22	U28、U29	Rclamp0514M.TBT	ESD protection device of HDMI
24	U30	ANX9011L	HDMI digital signal decode
25	U31	PI5C3306LE	(SDA, SCL) used for program update
26	U33	TDA8944J	Audio amplifier (BTL output)
27	U37	74HC4053D	Audio input switch
28	U38	PT2328	Video input switch

2. Function introduction of ICs or functional module of LCD TV with LS01chassis

1. Tuner (JS-6G1/111A25-A2)

Pin No.	Definition of pin	Function description
1	VCC	+5V power
2	BT	No connection
3	VCC	+5V power
4	SCL	IIC bus (clock)
5	SDA	IIC bus (data)
6	AS	Ground
7	AFS	Ground
8	NC	No connection
9	NC	No connection
10	NC	No connection
11	SIF/Out	Sound intermediate Frequency output
12	Video/Out	CVBS signal output
13	VCC (+5V)	+5V power
14	Audio/Out	Audio signal output

2. Image processing IC SVP-CX32LF

The SVPTMCX video processor is a highly integrated system-on-a-chip device, targeting the converging HDTV ready and PC-ready LCD TV, PDP TV applications where high precision processing of video and data are the requirements. SVPTMCX contains 6th generation dual-purposed triple 10-bit high-precision and high speed video ADCs for both PC and video inputs, the high-performance multi-format 3D digital comb video decoder that supports NTSC, PAL, and SECAM*, a HDTV sync separator, motion adaptive de-interlacing engine, and the video format conversion engine, supporting multi-window display in many different output modes. Trident's DCReTM – Digital Cinema Reality engine, is integrated inside the SVPTMCX family to provide the most natural cinema-realistic images. The DCReTM technology integrates advanced 3D-comb video decoding, advanced motion adaptive de-interlacing, object-based digital noise reduction, advanced 6th generation scaler, film mode support, average picture level (APL), edge smoothing and dynamic sharpness enhancement. Trident's patented Unified Memory Architecture (UMA) that allows frame rate conversion, 3D comb video decoding, and video enhancement processing to share the same memory buffer that is made up of high-speed and cost-effective PC graphic memory. All these advanced digital processing techniques combined with a true 10-bit video data processing for the most optimal video fidelity to provide the most natural and cinema quality video images. Designed for maximum system design flexibility, SVPTMCX integrates all video interfaces to support converging digital video, analog video, and PC data applications. The users of Trident's single chip SVP™CX series video processor(s) will benefit from many features while maintaining a price competitive advantage over the existing solution(s)

Main features:

- Integrated 6th Generation Motion and Edge Adaptive De-interlacing
- Integrated ADC
- PC auto tune
- Built-in 8-bit LVDS Transmitter
- 6th generation cubic-4 image scaling engine
- Advanced Chroma Processing and Dynamic Contrast Function
- Green color stretch, blue color stretch, skin color enhancement
- Integrated 6th Generation Motion Adaptive 3D Digital Comb Video Decoder with Programmable Filter
- 60Hz~100Hz interlaced scanning and 50Hz~75Hz progressive scanning
- Frame rate conversion
- 14D: dynamic picture enhancements
- Advanced Film Mode Recovery-3:2/2:2 pull down
- Build-in A/D conversion function
- Teletext function

- Supports 16/32bits SDRAM memory interface
- Multi-screen display mode
- OSD and VBI/Closed caption and advanced OSD engine

Pin function description:

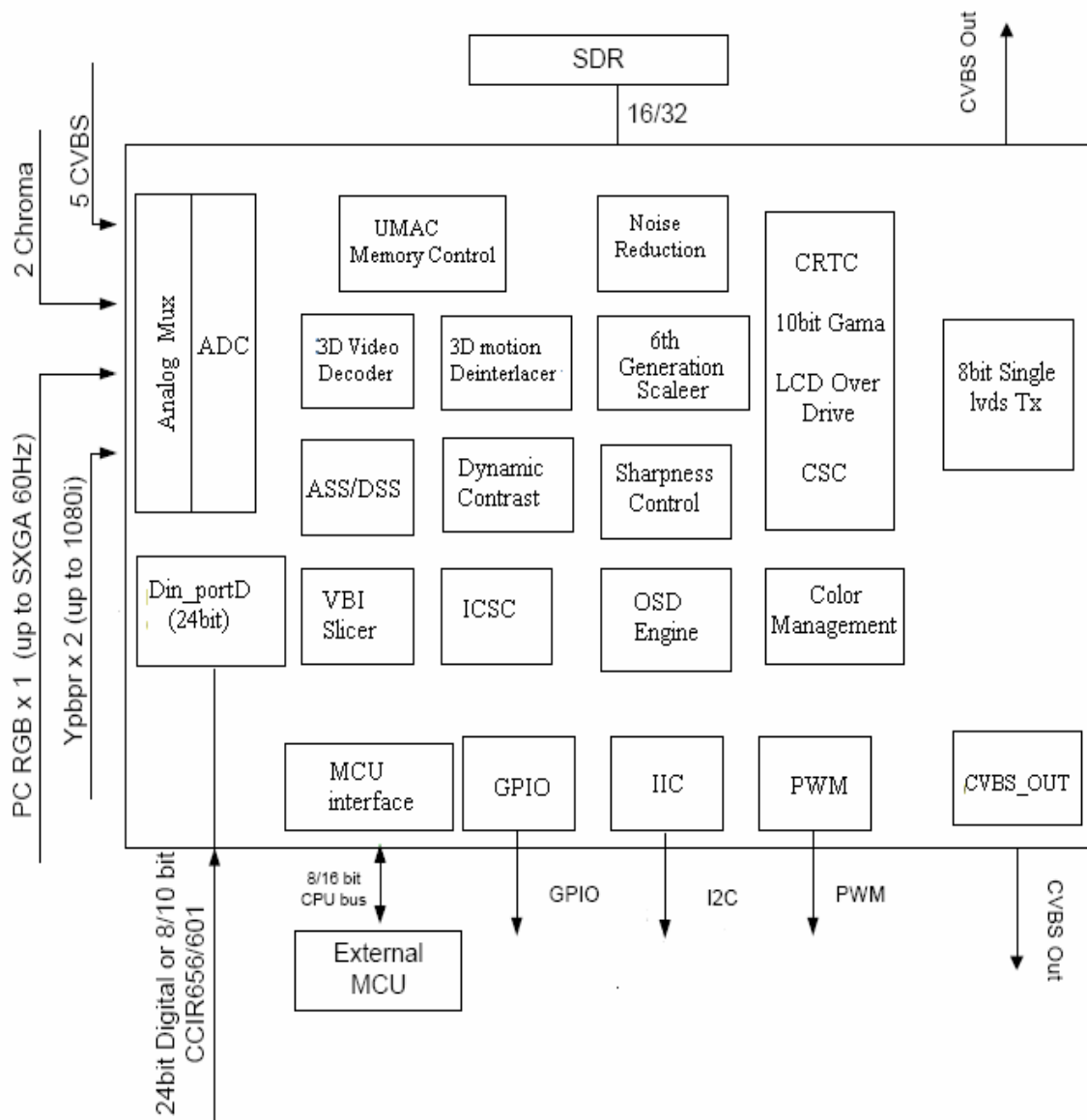
Pin No.	Designation of pin	Function of pin
Analog signal input/output terminal		
169	CVBS1	CVBS input 1
180	Y_G1	Y input
181	Y_G2	SCART1 Green signal input
182	Y_G3	S-Video Y signal input
183	PC_G	PC Green signal input
188	PR_R1	DVD interface Pr signal input
189	PR_R2	SCART1 Red signal input
190	PR_R3	SCART2 Y signal input
191	PC_R	PC Red signal input
192	C	S-Video C signal input
196	PB_B1	DVD interface Pb signal input
197	PB_B2	SCART1 Blue signal input
198	PB_B3	SCART1 CVBS signal input
199	PC_B	PC blue signal input
171	FS1	No connection
170	FS2	No connection
173	FB1	SCART1 RGB_FB signal input
172	FB2	SCART2 chroma signal input
174	VREFP_1	A/D conversion1 voltage reference +
175	VREFN_1	A/D conversion 1 voltage reference -
184	VREFP_2	A/D conversion 2 voltage reference +
185	VREFN_1	A/D conversion 2 voltage reference -
Digital signal terminal		
37	DP0	Digital signal I/O（DP0~DP23）interface
⋮	⋮	
29	DP8	
26	DP9	
25	DP10	
24	DP11	
22	DP12	
21	DP13	
18	DP14	
⋮	⋮	
14	DP18	
11	DP19	
⋮	⋮	
7	DP23	
CPU control terminal		
55	PWMO	Pulse width modulation input
57	SCL	IIC（clock）
58	SDA	IIC（data）
60	GPIO0	GPIO1 selection signal
59	GPIO1	GPIO2 selection signal
62	WR#	CPU write signal
63	RD#	CPU read signal
61	CS	CPU chip selection signal（low level effective）
56	INTN	Interrupt signal（low level effective）
84	ALE	Address latch signal
86	RESET	Reset signal (high level effective)
85	V5SF	SF Power（+5V）
4	DP_HS	Line synchronization signal

5	DP_VS	Field synchronization signal
23	DP_CLK	Digital port Clock
6	DP_DE_FLD	DE I/O terminal
64	ADDR0	CPU address（R0~R7）signal
⋮	⋮	
71	ADDR7	
83	A_D0	CPU address/data passage
⋮	⋮	
76	A_D7	
MISC port control signal		
162	CVBS_OUT2	SCART2 interface CVBS signal output
163	CVBS_OUT1	SCART1 interface CVBS signal output
157	TEST_MODE	Test mode signal (grounding)
158	AIN_HS	Line synchronization signal
159	AIN_VS	Field synchronization signal
205	XTALI	Crystal oscillator interface
204	XTALO	
SDRM controlling port		
124	MA0	Memory address（A0~A11）
⋮	⋮	
121	MA3	
118	MA4	
⋮	⋮	
113	MA9	
125	MA10	
126	MA11	
156	DQM0	Memory read/write byte signal
133	DQM1	
109	DQM2	
87	DQM3	
128	BA0	Memory stack address selection
127	BA1	
130	RAS#	RAS signal
131	CAS#	CAS signal
132	WE#	Memory write pulse
112	CLKE	Memory clock pulse
129	CS0#	Memory chip selection signal
111	MCK	Memory clock signal
155	MD0	Memory data interface
⋮	⋮	
148	MD7	
145	MD8	
⋮	⋮	
138	MD15	
107	MD16	
⋮	⋮	
100	MD23	
95	MD24	
⋮	⋮	
88	MD31	
LVDS port		
52	LVDS_VDDP	Power for LVDS
38	PLL_GND	PLL ground
39	PLL_VCC	PLL power
47	LVDSGND	LVDS ground
46	LVDSVCC	Power for LVDS
43	TCLK1M	Positive/Negative LVDS differential clock output

42	TCLK1P	Positive/Negative LVDS differential data output
51	TA1 M	
50	TA1P	
49	TB1M	
48	TB1P	
45	TC1M	
44	TC1P	
41	TD1M	
40	TD1P	
Clock and power		
146	VDDM	Memory port digital power
134	VDDM	
108	VDDM	
98	VDDM	
72	VDDH	3.3V power supply
19	VDDH	
160	VDDC	1.8V power supply
136	VDDC	
119	VDDC	
96	VDDC	
74	VDDC	
53	VDDC	
27	VDDC	
12	VDDC	
13	VSSC	Digital ground
28	VSSC	
54	VSSC	
75	VSSC	
97	VSSC	
120	VSSC	
137	VSSC	
161	VSSC	
20	VSSH	
73	VSSH	
99	VSSM	
110	VSSM	
135	VSSM	
147	VSSM	
195	AVDD3_ADC2	ADC analog power (+3.3V)
168	AVDD3_ADC1	
2	PLF2	Video PLL clock low pass filtering
207	MLF1	Memory PLL clock low pass filtering
1	PAVSS2	PLL ground
3	PAVDD2	PLL power (+1.8V)
206	PAVSS1	PLL digital ground
208	PAVDD1	PLL digital ground power (+1.8V)
203	PAVSS	PLL Digital ground
202	PAVDD	PLL digital ground power(+1.8V)
201	PDVSS	PLL Digital ground
200	PDVDD	PLL digital ground power (+1.8V)
177	AVDD_ADC1	ADC analog power (+1.8V)
186	AVDD_ADC2	
193	AVDD_ADC3	
178	AVDD_ADC4	
176	AVSS_ADC1	ADC analog ground
187	AVSS_ADC2	
194	AVSS_ADC3	
179	AVSS_ADC4	

165	AVDD3_OUTBUF	+3.3V analog power
164	AVSS_OUTBUF	
166	AVDD3_BG_ASS	Analog ground
167	AVSS_BG_ASS	

SVP-CX32LF internal block diagram:



3. T5BS4-9999 brief introduction:

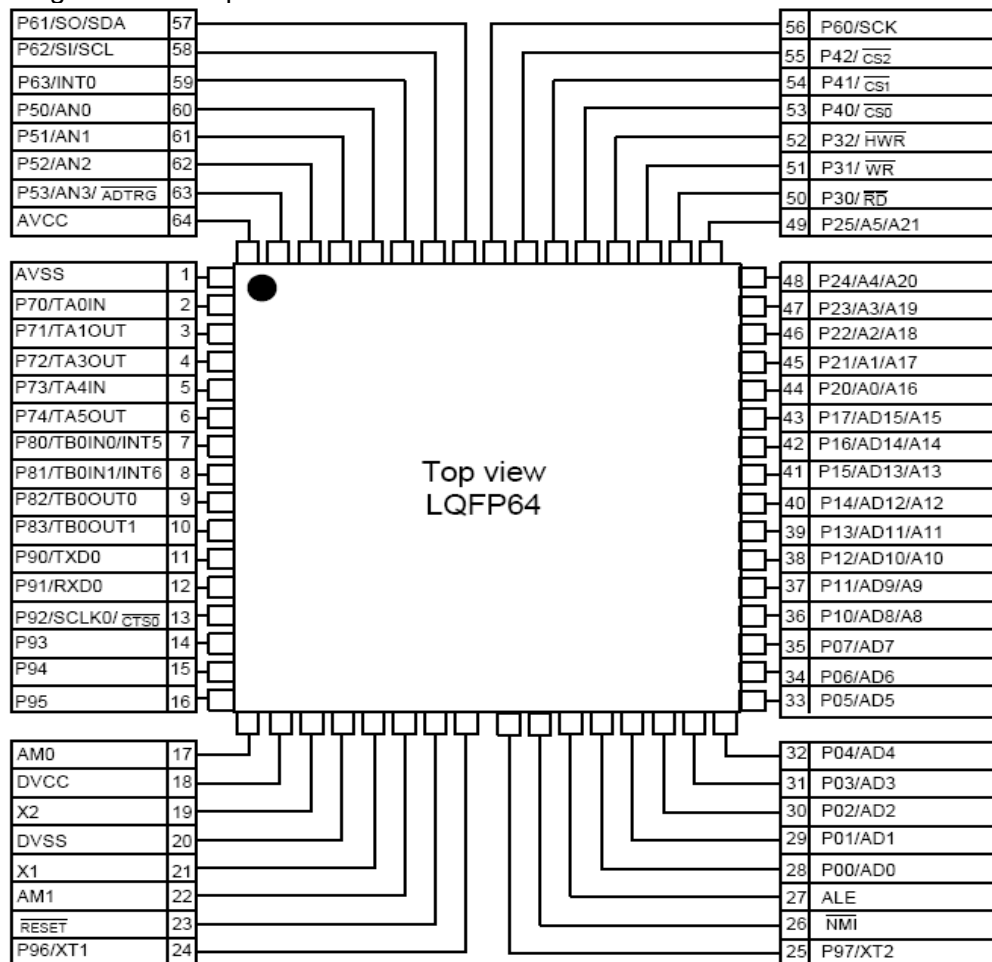
T5BS4-9999 is a high-speed 16-bit micro-controller designed for the control of various mid- to large-scale equipment. T5BS4-9999 is ROM-less product, T5BS4-9999 comes in a 64-pin flat package. Listed below are the features that is used for the control of a variety of small to large devices. T5BS4-9999 could extend ROM ,64 pins and is packaged in PLCC. It is the main control IC of the TV via I²C bus.

Main features:

- High speed 16-bit CPU (900/L1 CPU)
- Minimum instruction execution time: 148ns
- Build-in RAM: 10Kbytes
- Expandable up to 16Mbytes
- simultaneously support 8-/16-bit width external data bus
- 8-bit timers: 6 channels, 16-bit timers: 1 channel

- General-purpose serial interface: 1 channel
- Serial bus interface: 1 channel
- 10 bit A/D conversion interface: 4 channels
- Watchdog timer
- Timer for real time clock (RTC)
- Chip select/wait controller: 4 blocks
- 34 interrupt signals output
9 CPU interrupt, 21 internal interrupt, 4 external interrupt
- 53 I/O pins
- Standby function
- Clock control
fs=32.768KHz real-time time of time conversion function high frequency fc to fc/16
- Working voltage
When fc=27 MHZ, VCC=2.7~3.6V, when fc=10MHZ, VCC=1.8V to 3.6V
- 64 pin package (P-LQFP64-1010-0.50D standard)

Pin assignment description:

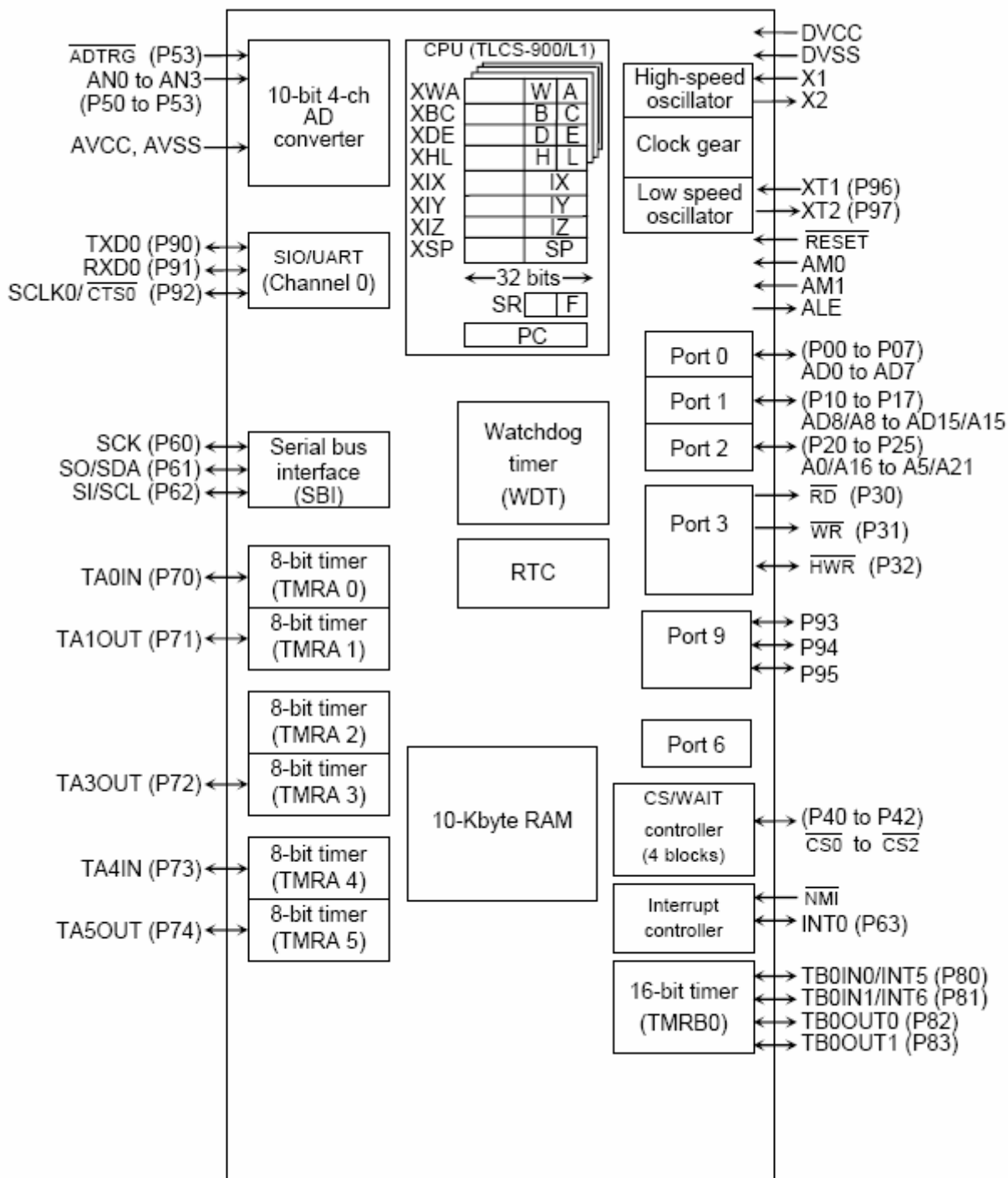


Pin introduction:

Pin	Designation	Function description
1	AVSS	Analog ground
2	P70/TA0IN	I ² C data input
3	P71/TA1OUT	I ² C clock output
4	P72/TA3OUT	PAGE signal output
5	P73/TA4IN	+5V power
6	P74/TA5OUT	Backlight on/off control
7	P80/TB0IN0/INT5	Remote control signal

8	P81/TB0IN1/INT6	+1.8V power supply
9	P82/TB0OUT0	Remote red control signal
10	P83/TB0OUT1	Remote green control signal
11	P90/TXD0	Digital ground
12	P91/RXD0	HDMI identity signal
13	P92/SCLK0/ $\overline{CTS0}$	No connection
14	P93	CON4(10 th pin)
15	P94	CON4(4 th pin)
16	P95	CON4(3 rd pin)
17	AM0	Bus byte selection
18	DVCC	+3.3V power
19	X2	Crystal oscillator interface
20	DVSS	Ground
21	X1	Crystal oscillator interface
22	AM1	Bus byte selection
23	$\overline{RESET}$	CPU reset control port
24	P96/XT1	Low frequency oscillation input interface
25	P97/XT2	Low frequency oscillation output interface
26	NMI	Interrupt request signal
27	ALE	Address latch pulse
28	P00/AD0	0~7 bit address/data port
⋮	⋮	
35	P07/AD7	
36	P10/AD8/A8	8~15 bit address/data port or 8~15 bit address port
⋮	⋮	
43	P17/AD15/A15	
44	P20/A0/A16	8~5 bit address port or 8~21 bit address port
⋮	⋮	
49	P25/A5/A21	
50	P30/ $\overline{RD}$	External memory read control terminal
51	P31/ $\overline{WR}$	External memory write control terminal (AD0~AD7)
52	P32/ $\overline{HWR}$	Data write control terminal (AD8~AD15)
53	P40/ $\overline{CS0}$	Internal address selection signal
54	P41/ $\overline{CS1}$	
55	P42/ $\overline{CS2}$	
56	P60/SCK	(no connection)
57	P61/SO/SDA	I ² C data
58	P62/SI/SCL	I ² C clock
59	P63/INT0	Interrupt request signal
60	P50/AN0	KEY signal port
61	P51/AN1	
62	P52/AN2	SCART1 FS signal
63	P53/AN3/ $\overline{ADTRG}$	SCART2 FS signal
64	AVCC	Analog power (+3.3V)

T5BS4-9999 internal functional block diagram:



4. STV-8217/STV-8218 brief introduction

STV-8217/STV-8218 main features:

■ Full-Automatic Multi-Standard Demodulation

- B / G / I / L / D / K / M / N Standards
- Mono AM and FM
- FM 2-Carrier and NICAM/BTSC

■ Sound Processing: Loudspeaker

- ST royalty-free processing: ST WideSurround, ST OmniSurround (Virtual Dolby Surround and
- Independent Volume / Balance

- Smart Volume Control (SVC), 5-band equalizer and Loudness

■ Analog Audio Matrix

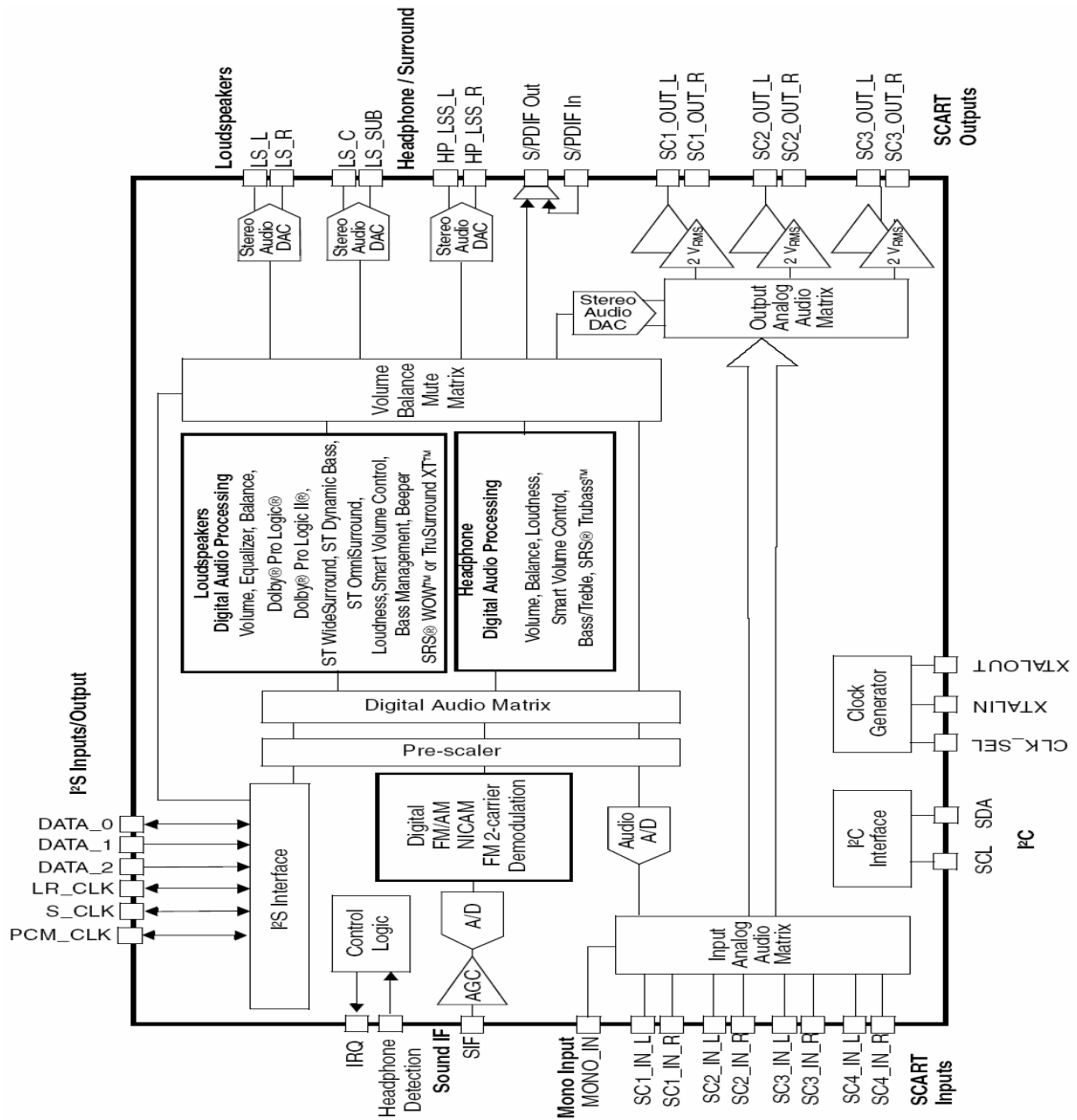
- 4 stereo inputs
- 3 stereo outputs
- THRU mode
- 2 VRMS capability

Pin introduction:

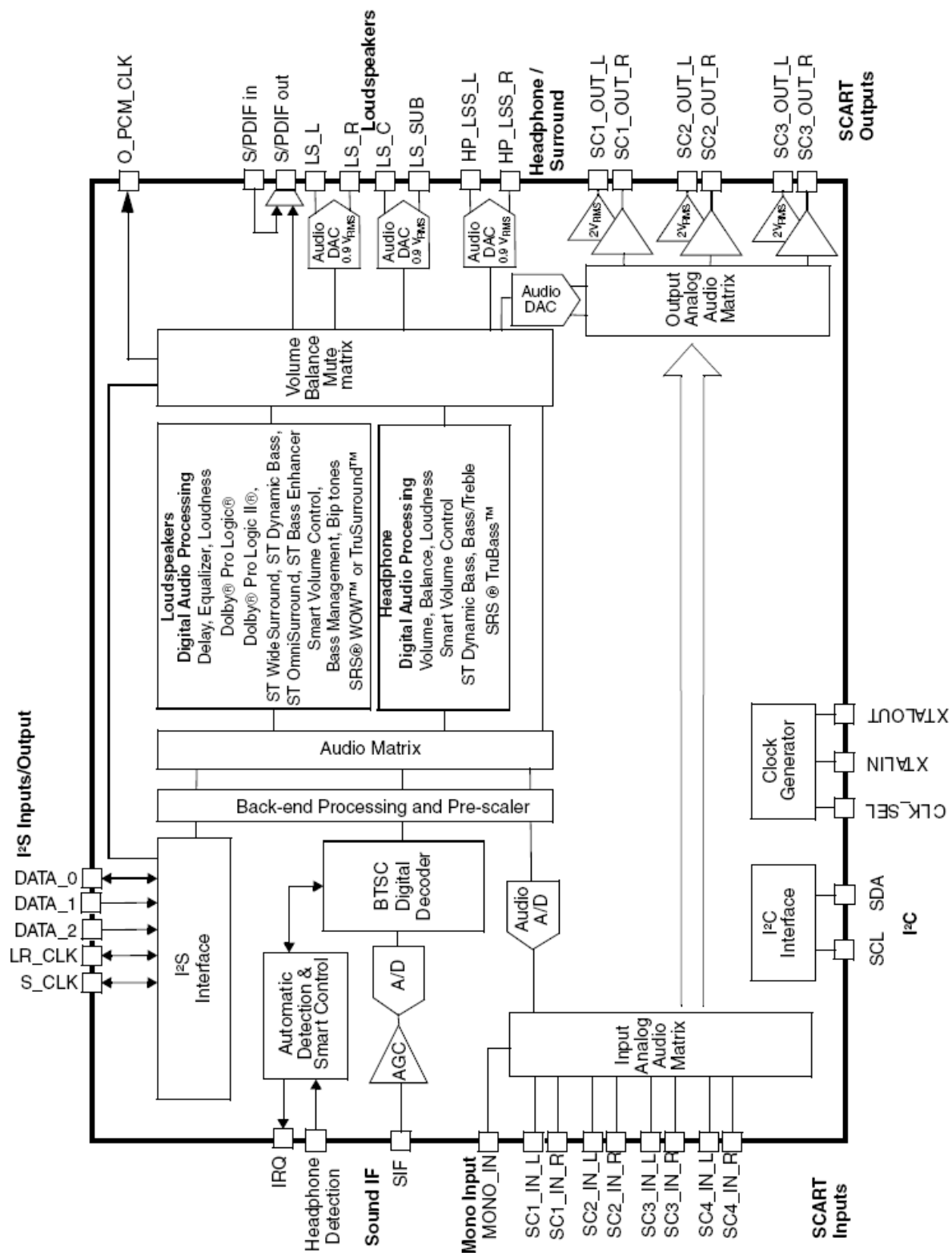
Pin	Designation	Function description
1	SC1_OUT_L	SCART1 audio output left
2	SC1_OUT_R	SCART1 audio output right
3	VCC_H	+8V power
4	GND_H	ground
5	SC3_OUT_L	SCART3 audio output left
6	SC3_OUT_R	SCART3 audio output right
7	VCC33_SC	+3.3V power
8	GND33_SC	Ground
9	SC1_IN_L	SCART1 audio output left
10	SC1_IN_R	SCART1 audio output right
11	VREFA	Audio bias voltage decoupling interface
12	GND_SA	Ground
13	VBG	Audio bias voltage decoupling interface
14	SC2_IN_L	SCART2 audio input left
15	SC2_IN_R	SCART2 audio input right
16	VCC33_LS	DACs power(+3.3V)
17	GND33_LS	DACs ground
18	SC2_OUT_L	SCART2 audio output left
19	SC2_OUT_R	SCART2 audio output right
20	VCC_NISO GND_SA	Polarization of the NISO (+3.3V) DACS ground
21	VSS33_CONV	DAC ground
22	VDD33_CONV	DAC power (+3.3V)
23	SC3_IN_L	SCART3 audio input left
24	SC3_IN_R	SCART3 audio input right
25	SCL_FLT	SCART channel filtering left
26	SCR_FLT	SCART channel filtering right
27	LS_C	No connection
28	LS_L	Left loudspeaker output
29	LS_R	Right ludspeaker output
30	LS_SUB	No connection
31	HP_LSS_L	No connection

32	HP_LSS_R	No connection
33	VSS18_CONV	DAC/ADC ground
34	VDD18_CONV	DAC/ADC power (8V)
35	/HP_DET	Earphone detection
36	ADR_SEL	hardware address selection for IIC bus
37	VSS18	Digital ground
38	VDD18	+1.8V power
39	SCL	I ² C bus clock
40	SDA	I ² C bus data
41	VSS18	Digital ground
42	VDD18	+1.8V power
43	/RST	Reset signal input/output terminal
44	S/PDIF_IN	No connection
45	S/PDIF_OUT	No connection
46	VDD33_IO1	+3.3V power
47	VSS33_IO1	Digital ground
48	CK_TST_CTRL	Digital ground
49	VSS18	Digital ground
50	VDD18	+1.8V Power
51	CLK_SEL	Clock input format selection
52	XTALIN_CLKXTP	Oscillator interface
53	XTALOUT_CLKXTM	
54	VCC18_CLK1	1.8V for clock PLL
55	GND18_CLK1	Ground
56	GND18_CLK2	Ground
57	VCC18_CLK2	+1.8V Power
58	VSS33_IO2	Digital ground
59	VDD33_IO2	+3.3V Power
60	I2S_PCM_CLK	No connection
61	I2S_SCLK	I ² S clock I/O channel1,2,3
62	I2S_LR_CLK	I ² S selection signal input/output
63	I2S_DATA0	I ² S bus data input/output stereo channel 1
64	I2S_DATA1	I ² S bus data input stereo channel 2
65	I2S_DATA2	I ² S bus data input stereo channel 3
66	VDD18	+1.8V Power
67	VSS18	Ground
68	BUS_EXP	Bus-expander function
69	IRQ	No connection

70	GND_PSUB	Ground
71	VDD18_ADC	+1.8V Power
72	VSS18_ADC	Ground
73	SIF_P	Sound IF input (positive terminal)
74	SIF_N	Sound IF input (negative terminal)
75	GNDPW_IF	Ground
76	VCC18_IF	+1.8V Power
77	GND18_IF	Ground
78	MONO_IN	Mono input
79	SC4_IN_L	SCART4 audio input left
80	SC4_IN_R	SCART4 audio input right



STV-8218 internal block diagram:



5. TDA8944J brief introduction:

The TDA8944J is a dual-channel audio power amplifier with an output of 2* 7 W at an 8 Ω load and a 12 V supply. The circuit contains two Bridge Tied Load (BTL) amplifiers with an all-NPN output stage and standby/mute logic. The TDA8944J comes in a 17-pin DIL-bent-SIL (DBS) power package. The TDA8944J is printed-circuit board (PCB) compatible with all other types in the TDA894x family. One PCB footprint accommodates both the mono and the stereo products.

main features:

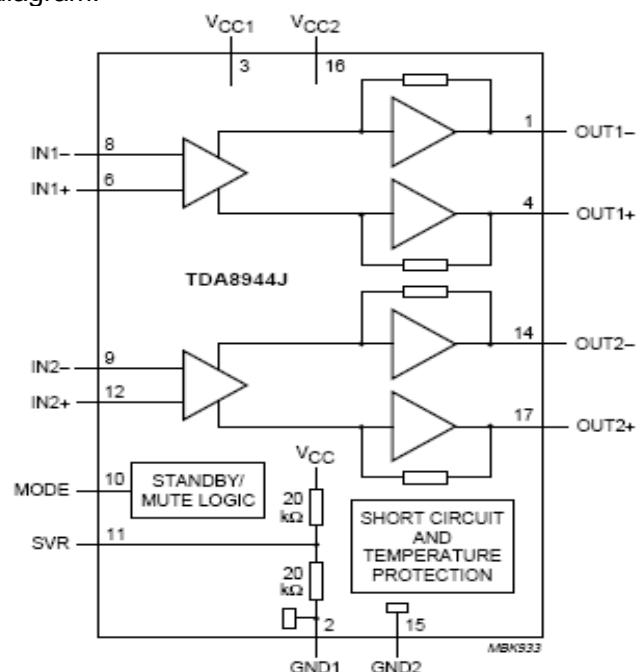
- High integration
- Standby and mute mode

- No on/off switching pops
- High supply voltage ripple rejection
- Low standby current
- Outputs short-circuit protected to ground, supply and across the load
- Overheat protection
- Linear output to drive external earphone, PC and portable audio equipment

Pin introduction:

Pin	Designation	Function description
1	OUT1-	negative loudspeaker terminal1
2	GND1	Ground
3	VCC1	+12V Power
4	OUT1+	positive loudspeaker terminal 1
5	N.C.	No connection
6	IN1+	Positive pole input 1
7	N.C.	No connection
8	IN1-	Negative pole input 1
9	IN2-	Negative pole input 2
10	MODE	Mode selection input (standby, mute, operating)Operation mode selection (standby, mute, work)
11	SVR	Half supply voltage decoupling (ripple rejection)Voltage decoupling filtering (grounding)
12	IN2+	Positive pole input terminal 2
13	N.C.	No connection
14	OUT2-	Negative loudspeaker terminal 2
15	GND2	Ground
16	VCC2	+12V Power
17	OUT2+	Positive loudspeaker terminal 2

TDA8944J internal block diagram:



6. ANX9011L brief introduction:

The ANX9011 is an advanced multimedia receiver compliant with High Definition Multimedia Interface (HDMI) Specification 1.1. HDMI is the first transport standard to unify digital video, audio, and control data over low - cost cables. It connects digital television, flat panel displays and project systems digitally to multimedia sources: DVD players, high definition set - top boxes, digital video tape recorders, and personal computers. Digital transmission, in turn, delivers an uncompromising

multimedia experience. HDMI also includes encryption for premium contents pursuant to the High - bandwidth Digital Content Protection (HDCP) standard. The ANX9011 embeds the HDCP keys and key selection vectors to reduce manufacturing complexity and system cost.

Features:

- Single HDMI receiver supporting link data rate up to 165 MHz
- HDMI 1.1,HDCP 1.1 and DVI 1.0 compliant
- WideEye architecture for signal conditioning and equalization
- Support multi-format video processing
 - 24 bit RGB / YCbCr 4:4:4
 - 16/20/24 bit YCbCr 4:2:2
 - 8/10/12 bit YCbCr 4:2:2 (ITU BT - 656)
 - 12bit double data rate interface
 - 24/48 bit single data rate interface
- Color space conversion: RGB to/from YCbCr both directions
- Auto video mode configuration
- Digital audio interface
 - 32-192kHz audio sampling rate
 - Provide 4-channel IIS interface for 8 audio channels
 - Mute software configuration
- Integrated HDCP decryption engine and pre - programmed keys
- Supports automated link integrity checking
- Programmable power management with automatic shutdown for power conservation
- 128 pin LQFP packaging

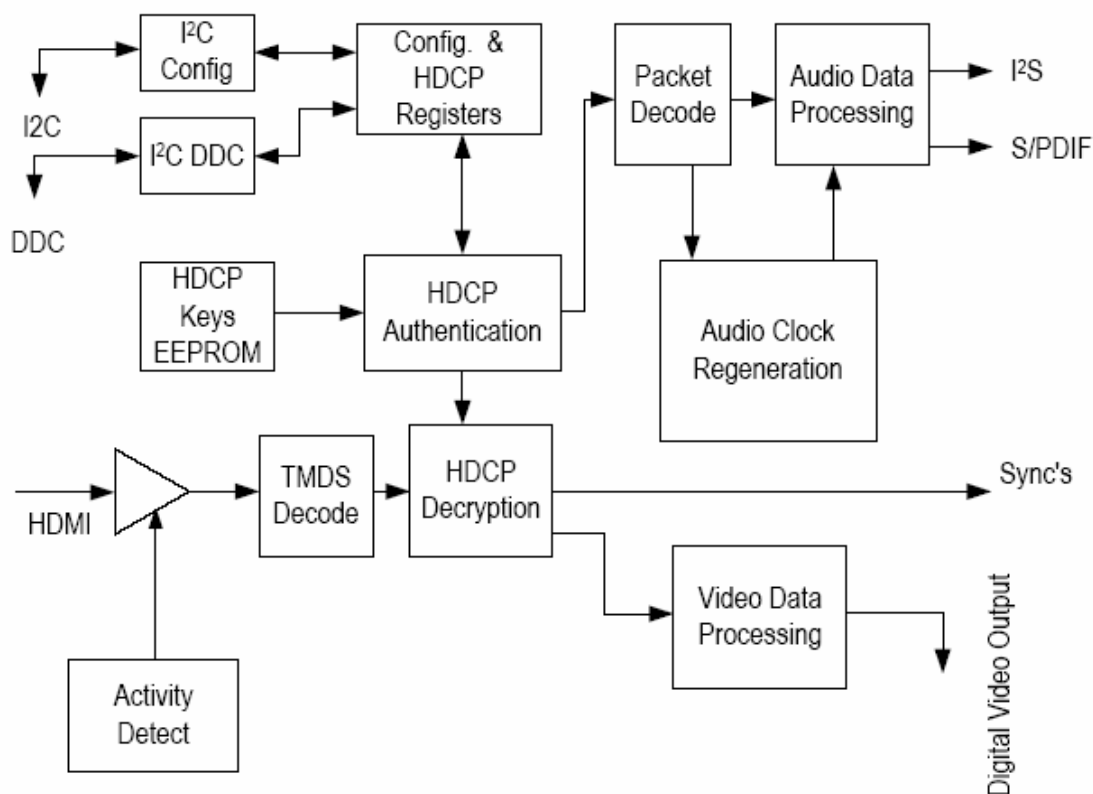
Pin function

Pin	Designation	Function description
Digital image output terminal		
92	VDE23	24bit (DP0~DP23) digital video output data bus
⋮	⋮	
96	VDE19	
99	VDE18	
⋮	⋮	
101	VDE16	
⋮	⋮	
105	VDE12	
108	VDE11	
⋮	⋮	
117	VDE4	
121	VDE3	
⋮	⋮	
124	VDE0	
2	VDO23	24bit (QO0~QO23) no connection
⋮	⋮	
5	VDO20	
8	VDO19	
⋮	⋮	
11	VDO16	
14	VDO15	
⋮	⋮	
17	VDO12	
20	VDO11	
⋮	⋮	
23	VDO8	
26	VDO7	

⋮	⋮	
29	VDO4	
32	VDO3	
⋮	⋮	
35	VDO0	
119	VD_CLK	Video output data clock
127	DE	Video output data effective level signal
128	HSYNC	Line synchronizing signal
1	VSYNC	Field synchronizing signal
Digital audio output terminal		
85	XTAL_IN	Crystal oscillator interface
84	XTAL_OUT	
79	MCLKOUT	Audio main control clock output
76	IIS_SCK	IIS bus clock
75	IIS_WS	IIS signal selection
74	IIS_SD0	IIS bus data
⋮	⋮	IIS channel selection (no connection)
71	IIS_SD3	
70	SPDIF	(no connection)
67	MUTEOUT	Mute control signal (no connection)
Control signal port		
91	INT	Interrupt request output
89	RESETN	Reset signal input
42	DDC_SCL	DDC Clock signal
41	DDC_SDA	DDC address/data signal
40	CFG_SCL	I ² C bus clock
39	CFG_SDA	I ² C address/data
90	HDMI_DET	Synchronization detection
38	DEVAD	I ² C connection detection signal
44	HDMI_5V	Cable insert detection terminal
88	RESDL	Ground
43	NC	No connection
45	NC	
HDMI 信号 input terminal		
51	HDMI_CLKP	Differential clock input
50	HDMI_CLKN	
55	HDMI_D0P	Differential data input1
54	HDMI_D0N	
59	HDMI_D1P	Differential data input 2
58	HDMI_D1N	
63	HDMI_D2P	Differential data input 3
62	HDMI_D2N	
Power and ground		
DVDD18	12, 24, 36, 51, 66, 81, 82, 112, 125	+1.8V digital Power
DVDD33	7, 19, 31, 68, 77, 98, 107, 120	+3.3V digital Power

AVDD33	47, 49, 53, 57, 61, 86, 87	+3.3V analog Power
DVSS	6, 13, 18, 25, 30, 37, 65, 69, 78, 80, 97, 106, 113, 118, 126	Digital ground
AVSS	46, 52, 56, 60, 64, 83	Analog ground

ANX9011L internal block diagram:



7. 74HCT4052D brief introduction:

74HCT4052D is a 4-channel bi-directional analog multiplexer and multi-channel output selector. Each multi-channel output selector has 4 independent input/output terminals and 1 common input/output terminal. It is often used in analog and digital multiplexing, and multi-channel output selecting circuit and signal control system.

Feature:

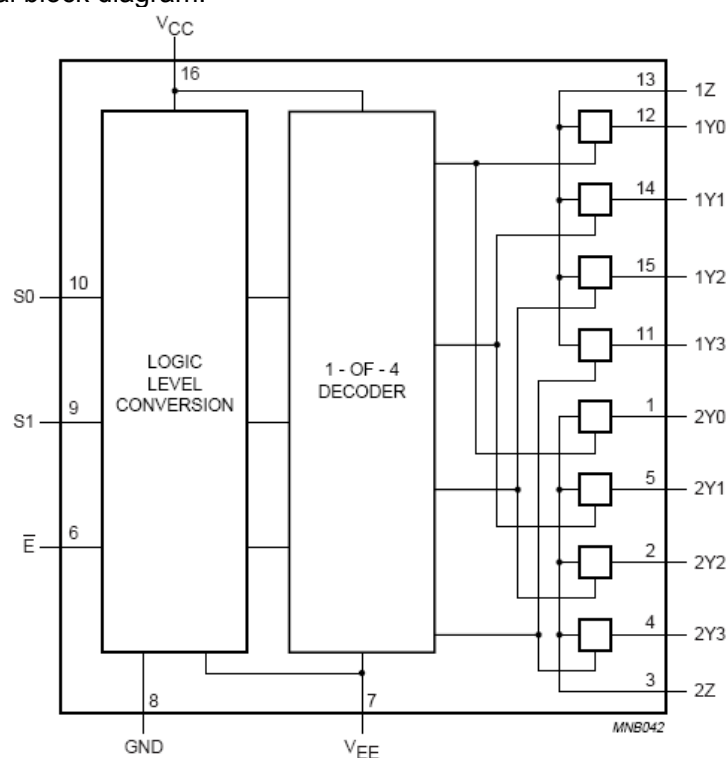
- -5V to +5V widely range Power input
- Low on-resistance
- Typical “break before make” built in
- Complies with JEDEC standard no. 7A
- ESD protection:
HBM EIA/JESD22-A114-B exceeds 2000 V
MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from -40 ° C to +85 ° C and -40 ° C to +125 ° C.
- Automatic protection function

Pin introduction:

Pin	Designation	Function description
1	2Y0	PC left audio input
2	2Y2	HD left audio input
3	2Z	Left audio input
4	2Y3	SCART2 left audio input
5	2Y1	AV left audio input

6	E	Ground
7	VEE	Ground
8	GND	Ground
9	S1	Select pulse input (+3.3V Power)
10	S0	
11	1Y3	SCART2 right audio input
12	1Y0	PC right audio input
13	1Z	Right audio output
14	1Y1	AV right audio input
15	1Y2	HD right audio input
16	VCC	+5V Power

74HCT4052D internal block diagram:

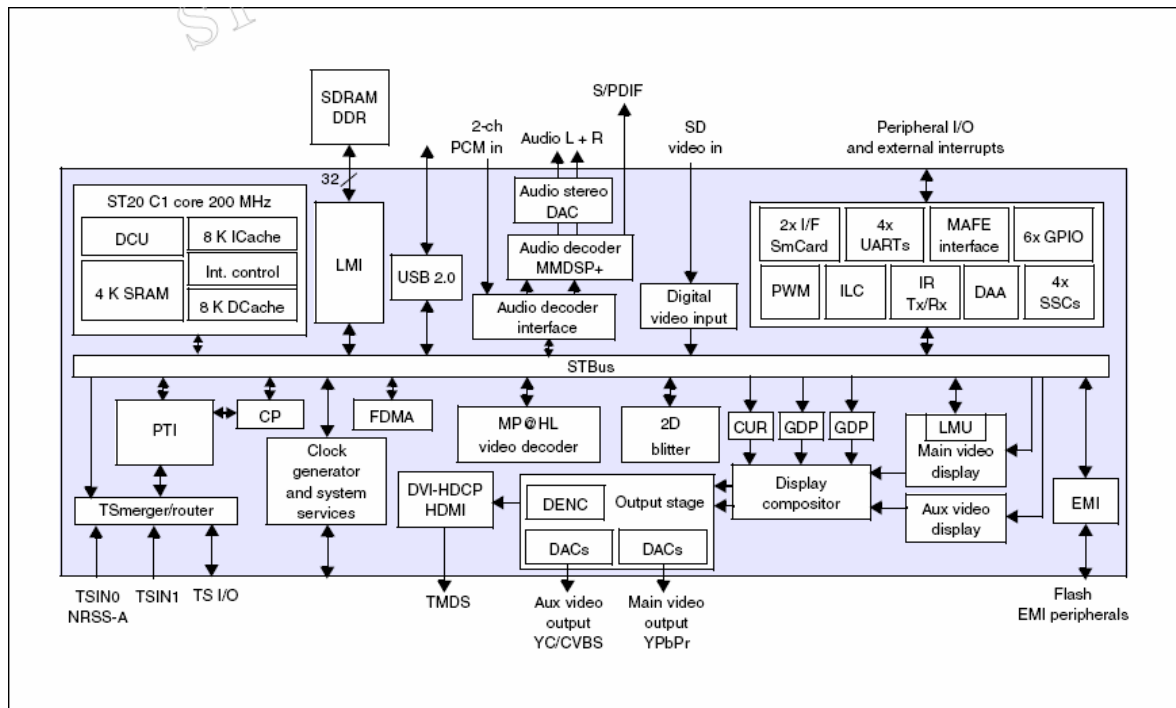


8. STI7710 brief introduction

FEATURES

- Enhanced ST20 32-bit VL-RISC CPU
 - 200 MHz, 8-Kbyte Icache, 8-Kbyte Dcache and 4-Kbyte SRAM
- Unified memory interface
- Dual transport stream merger – Supports DVB, DIRECTV®, and DCII
 - Integrates DES-ECB, DES-CBC, DVB, ICAM, XTV, Multi2 and Fast-I descramblers
 - NDS random access scrambled stream protocol (RASP) compliant
 - Low-cost DVB-CI and Cable Card support
- MPEG2 video decoder
 - Trick modes including smooth fast-forward and rewind
- Video encoder – Single multi format HD display
 - Supports 1080I, 720P, 480P and 480I resolution
 - Analog RGB or YPbPr HD output – HDMI encoding
 - Digital video HD output – Single SD display
 - Analog YPbPr, CVBS and Y/C SD output
- Copy protection
 - HDMI / HDCP copy protection hardware
 - Macrovision™ copy protection for 480I and 480P output

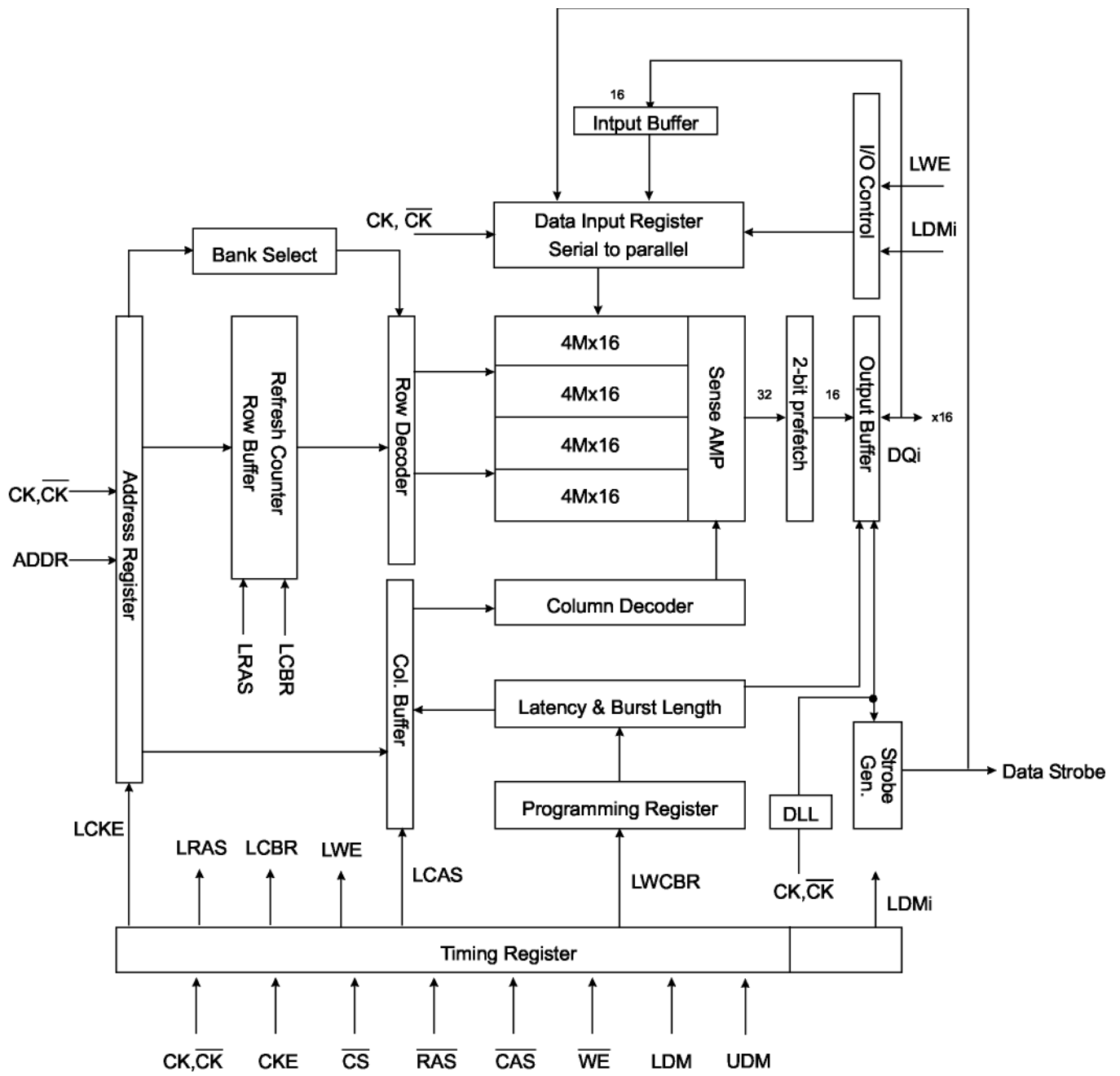
STI7710 internal block diagram:



9. K4D551638H brief introduction

- 2.6V + 0.1V power supply for device operation
- 2.6V + 0.1V power supply for I/O interface
- SSTL_2 compatible inputs/outputs
- 4 banks operation
- MRS cycle with address key programs
 - Read latency 3,4 (clock)
 - Burst length (2, 4 and 8)
 - Burst type (sequential & interleave)
- All inputs except data & DM are sampled at the positive going edge of the system clock
- Differential clock input
- No Write-Interrupted by Read Function
 - (WIR function can be supported only for 200/166MHz)
 - 2 DQS's (1DQS / Byte)
 - Data I/O transactions on both edges of Data strobe
 - DLL aligns DQ and DQS transitions with Clock transition
 - Edge aligned data & data strobe output
 - Center aligned data & data strobe input
 - DM for write masking only
 - Auto & Self refresh
- 64ms refresh period (8K cycle)
- 66pin TSOP-II lead free package(RoHS Compliant)
- Maximum clock frequency up to 250MHz
- Maximum data rate up to 500Mbps/pin

K4D551638H internal block diagram:



10. TDFS-G431D General specification

NO	ITEM	SPECIFICATIONS	NOTES														
1- 1	Input Frequency Range	VHF: 174MHz to 230MHz UHF: 470MHz to 860MHz	(NOTE1) (NOTE2)														
1- 2	Channel Bandwidth	UHF= 8MHz or 7MHz VHF= 8MHz or 7MHz															
1- 3	Channel Assignment	European , Australian Channel and ± 167KHz offset															
1- 4	Input Signal Level	-90dBm ~ -15dBm															
1- 5	Input Impedance	75Ω nominal															
1- 6	Loop Through Output Impedance	75Ω nominal															
1- 7	OFDM Demodulation IC	TDA10046HT / TDA10046AHT															
1- 8	OFDM Spectrum	2k, 8k -carrier and non-hierarchical, hierarchical(DVBT-T compliant)															
1- 9	Modulation Modes	QPSK, 16QAM, 64QAM															
1-10	Guard Interval Modes	1/32, 1/16, 1/8, 1/4 active symbol duration															
1-11	FEC Modes	Rate = 1/2, 2/3, 3/4, 5/6, 7/8															
1-12	Output Format	MPEG-2 Transport Stream (TTL-compatible)															
1-13	Control format	I ² C Bus Interface															
1- 14	Power Supply Voltages	<table><tr><th>Pin No</th><th>Name</th><th>Operating Supply Voltages</th></tr><tr><td>1</td><td>Ant Power</td><td>+5V ±0.25V DC</td></tr><tr><td>3</td><td>B1(+5V)</td><td>+5V ±0.25V DC</td></tr><tr><td>12</td><td>B2(+3.3V)</td><td>+3.3V ±0.15V DC</td></tr><tr><td>14</td><td>B3(+1.8V)</td><td>+1.8V ±0.1V DC</td></tr></table>		Pin No	Name	Operating Supply Voltages	1	Ant Power	+5V ±0.25V DC	3	B1(+5V)	+5V ±0.25V DC	12	B2(+3.3V)	+3.3V ±0.15V DC	14	B3(+1.8V)
Pin No	Name	Operating Supply Voltages															
1	Ant Power	+5V ±0.25V DC															
3	B1(+5V)	+5V ±0.25V DC															
12	B2(+3.3V)	+3.3V ±0.15V DC															
14	B3(+1.8V)	+1.8V ±0.1V DC															
1- 15	Temperature	Operating 0 ~ +60 °C Storage -10 ~ +70 °C															
1- 16	Humidity	Operating Less than 80 % RH (at40 °C) Storage Less than 95 % RH (at40 °C)															

TDFS-G431D Pin Description

Pin NO	Pin Name	PIN DESCRIPTION
1	Ant power	This terminal is used for active antenna power ON / OFF .
2	RF AGC	This terminal is used for the monitoring RF AGC voltage. N/C
3	B1(+5V)	Power Supply for the pre-amp.RF amp. PLL IC and IF amp.
4 . 6 . 13	GND	GND
5	TU T/P	. This terminal is used for the monitoring TU voltage. N/C
7	RESET	Resets the module to default configuration. Active low.
8	ERROR OUT	Transport stream error. The current packet contains uncorrectable error
9 . 10 . 11	N/C	N/C
12	B2(+3.3V)	Pad Power Supply for the OFDM IC.
14	B3(+1.8V)	Core Power Supply for the OFDM IC.
15	IF T/P	This terminal is used for the monitoring IF Response. N/C
16	PSYNC	Indicates the beginning of a transport package by asserting PSYNC during the sync byte of the message. Active high.
17	ENABLE	Indicates whether data word is enable data or padding packets. Active high.
18 ~ 25	DATA[7; 0]	An eight bit parallel port to output a transport packet data word The MPEG-2 transport stream is TTL compatible.
26	MCLK	The clock synchronizes the data stream. The clock signal is pulsed each time a valid data word is output on the DATA 0-7.
27	SDA	I2C Serial Data line
28	SCL	I2C Serial Clock Line

Chapter 3: Analysis of Signal processing Flowchart

This chapter mainly introduces the receipt and dispose of AV signal the power supply system and system control process of this TV. (Model of LT32GJ01E is taken as an example, other models is similar and will not be explained here for each. There are minor differences in power supply among different models of LCD screen; the details are shown in Specifications).

1. Video signal flow

RF signal is demodulated by tuner, then the obtained video signal and signals inputted from COMPONENT terminal, AV, S-VIDEO, 2-way SCART interface and VGA interface are all sent into video-processing IC SVP-CX32LF for decoding. The different format input signals are changed into uniform LVDS signals, and are sent to LCD screen. In addition, TV video signal is processed by SVP-CX32LF to generate 2 CVBS signal, which are used in SCART video output.

Signal inputted from HDMI interface is decoded into digital video signal BY ANX9011L, which is sent into video decoding IC SVP-CX32LF for decoding. After procession, the obtained uniform LVDS differential signal is sent into LCD Screen.

2. Sound process flow

RF signal is demodulated by tuner, and then the obtained SIF signal (SIF-2 signal) and audio signal inputted from Scart1 interface are directly processed by STV-8217. The output audio signal of STV-8217 is sent into power amplifier TDA8944J, and the amplified signal is finally sent into speaker or earphone.

Signals from HDTV terminal, AV terminal, Scart2 interface and PC Audio are first sent into 74HCT4052D for choosing passages, and then sent into STV-8217 for demodulation and sound process. The output audio signal of STV-8217 is sent into power amplifier TDA8944J, and finally the amplified signals are sent into speaker or earphone.

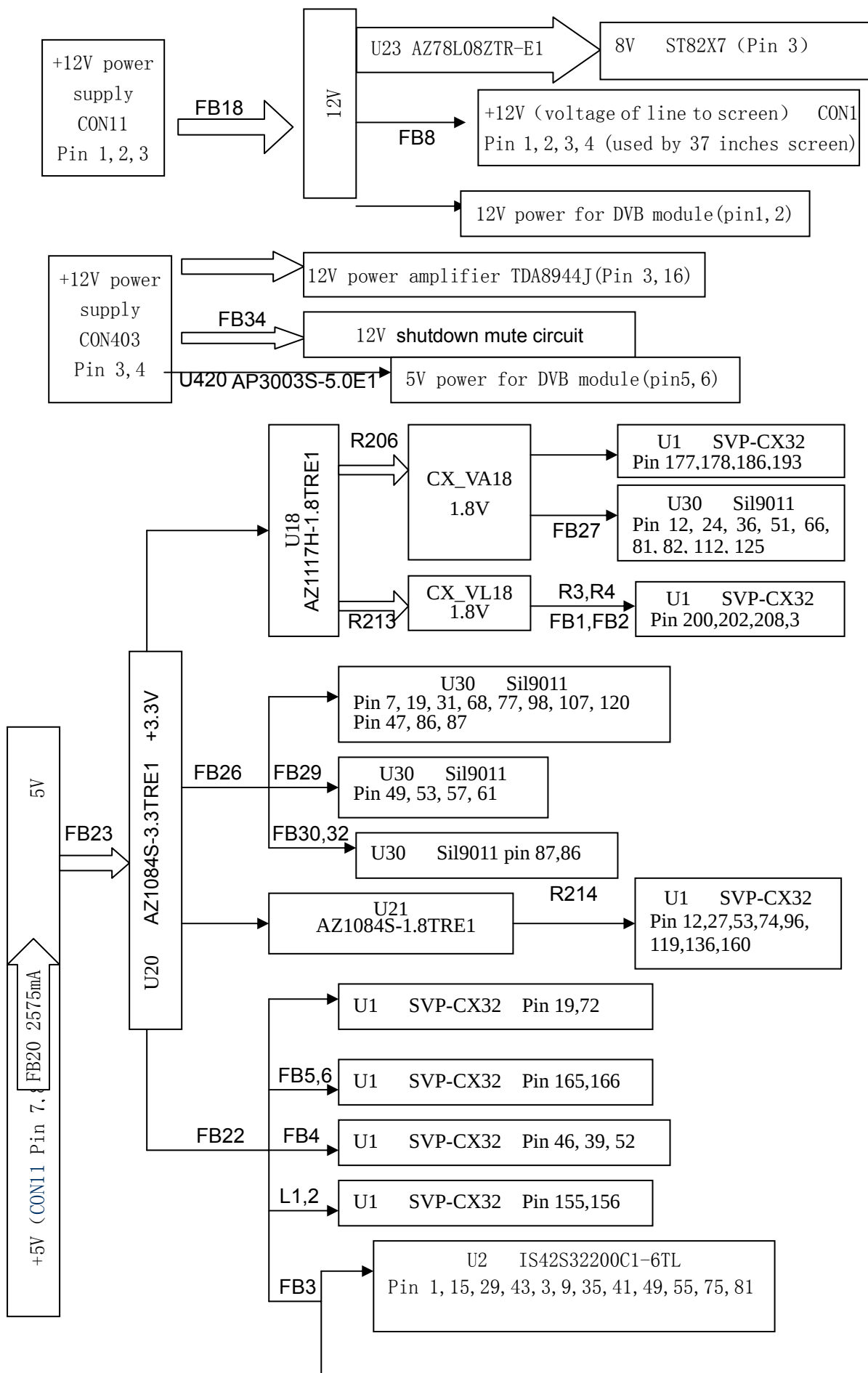
After the demodulation and sound effect processing of STV-8217, there is an audio output which is used for sound output of Scart1 terminal.

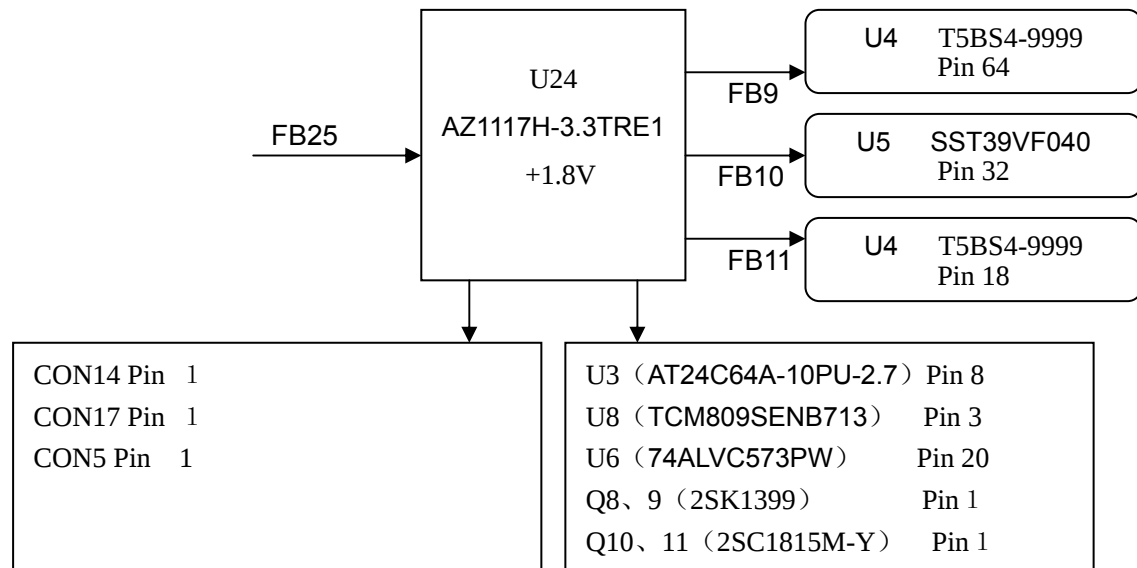
3. Power supply system

There are 4 ways of voltage output in the power panel: +24V (6A)、+12V (2A)、+5V (2A) and +5VS (1A) . +24V output is provided for LCD screen; +12V output is provided for power amplifier TDA8944J, and is also changed into +8V output by AZ78L08ZTR-E1 to supply STV-8217 IC; +5V output is changed into 1.8V output and 3.3V output by DC/DC (such as AZ1117H-1.8TRE1 and AZ1117H-3.3TRE1) to satisfy the needs ICs. +24V, +12V and +5V outputs will be cut off in standby state. While +5VS output is the power supply of MCU, infrared receiver and EEPROM etc, and will be cut off when the AC is turn off.

5V output will be divided into two ways: one way is changed into +3.3V and +1.8V analogue power supplies through DC/DC converter for STV-8217 IC, ANX9011LF IC etc and peripheral circuits; other way is changed into +3.3V and +1.8V digital power supplies through DC/DC converter for SVP-CX32 IC etc and peripheral circuits, and this way of 5V voltage will be cut off in standby state, while the other way of 5V voltage supply power especially for MCU, infrared receiver and EEPROM etc, and will still operating in standby state.

(1) The composition and distribution of the TV power supply





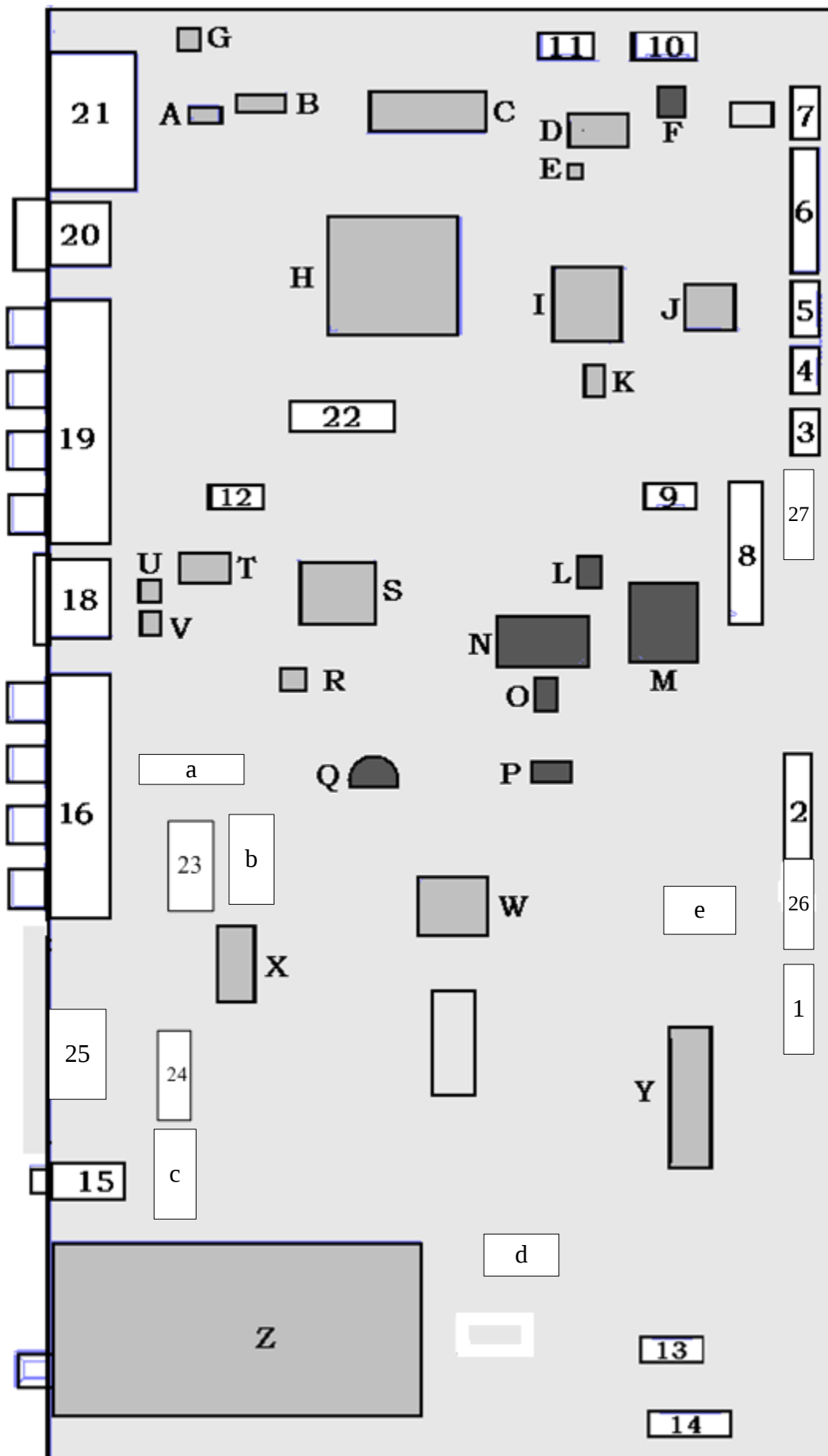
(2) Pin level schedule for Voltage regulators on mainboard

Position number	Component model	Pin 1(V)	Pin 2(V)	Pin 3(V)
U18、U22	AZ1117H-1.8TRE1	GND	1.8V	3.3V
U19、U24	AZ1117H-3.3TRE1	GND	3.3V	5V
U20	AZ1084S-3.3TRE1	GND	3.3V	5V
U21	AZ1084S-1.8TRE1	GND	1.8V	3.3V
U23	AZ78L08ZTR-E1	12V	GND	8V

(3) Pin sequence of power cord of power panel

Position number	Pin	Pin definition	Pin function description
CON1	1	ON/OFF	L: OFF ; H: ON
	2,3	GND	GND
	4,5	5V	+5V/4A
	6	5Vstb	+5V/1A
	7,8	GND	GND
	9,10	12V	+12V/1A
CON2	1,2	12VA	+12V/2A
	3,4,5,6	GND	GND
	7,8	24Vio	+24V/1A
CON3	1,2,3	GND	GND
	4,5,6	24VI	+24V/4A

4. Position and definition of the main components and sockets on mainboard(see next page)



(1) Socket definition

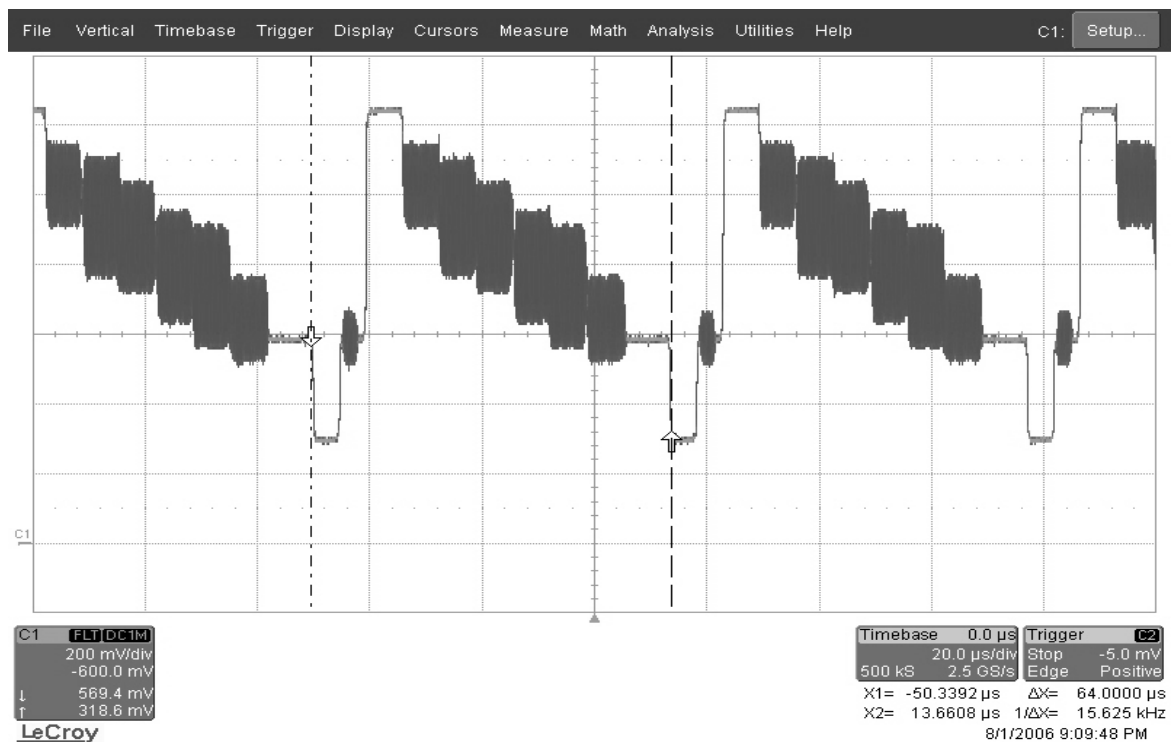
Serial number	Position number	Connecting object	Function description
1	CON403	Power panel	GND, GND, +12V, +12V
2	CON11	Power panel	+12V, +12V, +12V, GND, GND, GND, +5V, +5V, +5V, +5V
3	CON13	Back light control line	GND, GND, back light switch control, back light brightness control
4	CON14	Keyboard	+3.3V、GND、KEY1、KEY2
5	CON17	Remote control receiving board	+3.3V、REMOTE、GND、indicator1、indicator1
6	CON4	Standby	
7	CON5	Standby	
8	CON1	LVDS interface of line to screen	
9	CON15	I ² C	
10	CON12	Power panel	+5V_SB , +5V_SB , GND , GND , Power supply control
11	CON13	Standby	
12	CON8	Standby	
13	CON9	Speaker	L+,L-,R+,R-
14	CON10	Side AV board	
15	J9	VGA audio signal input	
16	J8	HD, audio, video signal input & output	
18	J4	HDMI input	
19	J2	HD, audio, video signal input	
20	J6	S terminal input	
21	J3	VGA input	
22	CON2	Standby	
23	CON22	DVB Y/Pb/Pr/L/R	For Asia market
24	CON24	DVB Cvbs/R/L	For Europe market
25	J10	RS232	For DVB Update
26	CON20	Power	12V,12V,GND,GND.5V,5V
27	CON21	I/O	

(2) Main components descriptions

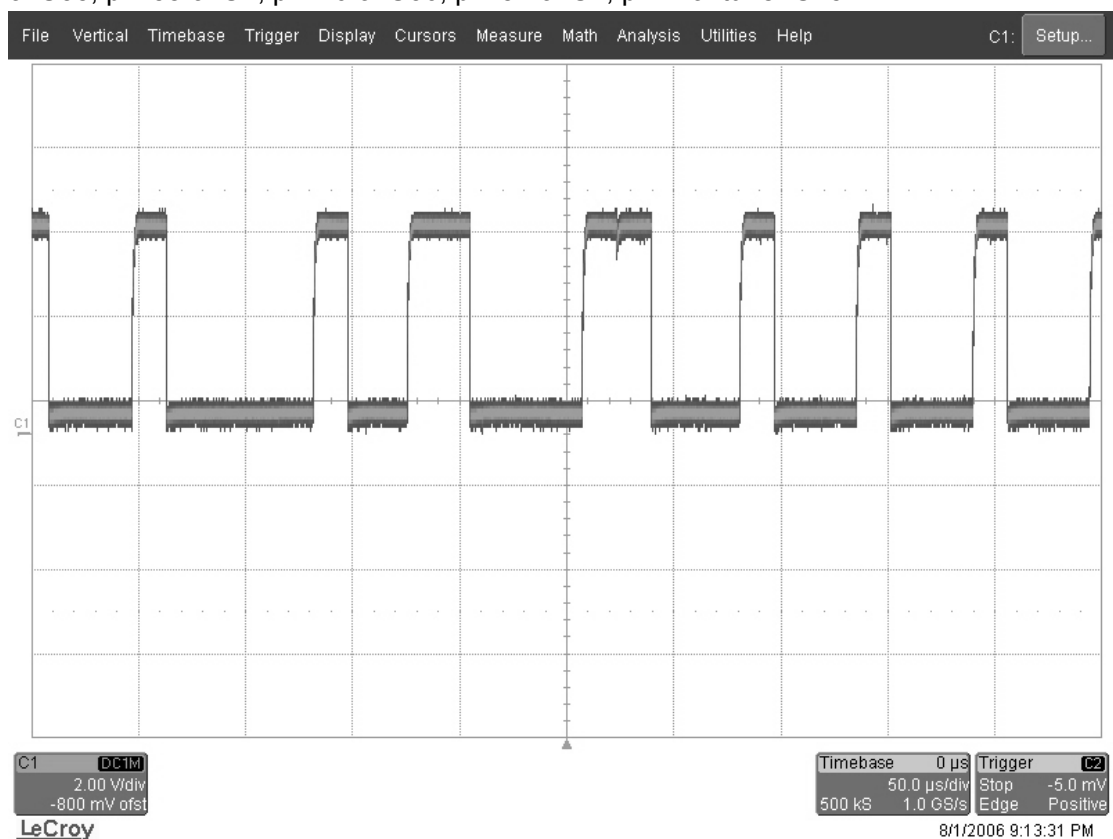
Serial number	Position number	component	Function description
A	U16	AT24C02BN-10SU-1.8	EEPROM
B	U14	74LVC14AD	VGA line and field synchronizing signal shaping
C	U2	IS42S32200C1-6TL	2MX32bits SDRAM
D	U3	AT24C64A-10PU-2.7	EEPROM
E	U8	TCM809SENB713	MCU reset IC
F	U31	PI5C3306LE	I ² C bus switcher for program upgrading
G	U1	SVP-CX32LF	Video decoding, image processor, A/D and D/A conversion
H	U5	SST39VF040-70-4C-NHE	Flash MEMORY , storing whole machine control program
I	U4	T5BS4-9999	MCU
J	U6	74ALVC573PW	Address latch, for latching and extending the address line
K	U18、U21、U22	AZ1117H-1.8TRE1	3.3V to 1.8V DC-DC Converter
L	U20	AZ1084S-3.3TRE1	5V to 3.3V DC-DC Converter
M	U19 、U24	AZ1117H-3.3TRE1	5V to 3.3V DC-DC Converter
O	U23	AZ78L08ZTR-E1	12V to 8V DC-DC Converter
R	U26	CS4344-CZZ	HDMI digital audio decoding and D/A conversion
T	U25	AT24C02BN-10SU-1.8	EEPROM
U/V	U28、U29	Rclamp0514M.TBT	HDMI signal ESD protective device
S	U30	ANX9011L	HDMI decoding, HDTV video/audio reproduction
X	U9	74HCT4052D	AV input sound passage switcher
U	U33	TDA8944J	2X7W Sound Amplifier (BTL Output)
Z	J11	JS-6G1/111A25-A2	Tuner
W	U35	STV-8217	Sound Processor
a	U38	PT2328	Video Switch
b	U37	74HC4053D	Sound Switch
c	U37	74HC4053D	Video and Sound Switch(only on Europe)
d	U39	AS7805DTR-E1	DC-DC Converter (12V to 5V)
e	U420	AP3003S-5.0E1	DC-DC Converter (12V to 5V)

5. Waveforms at key points

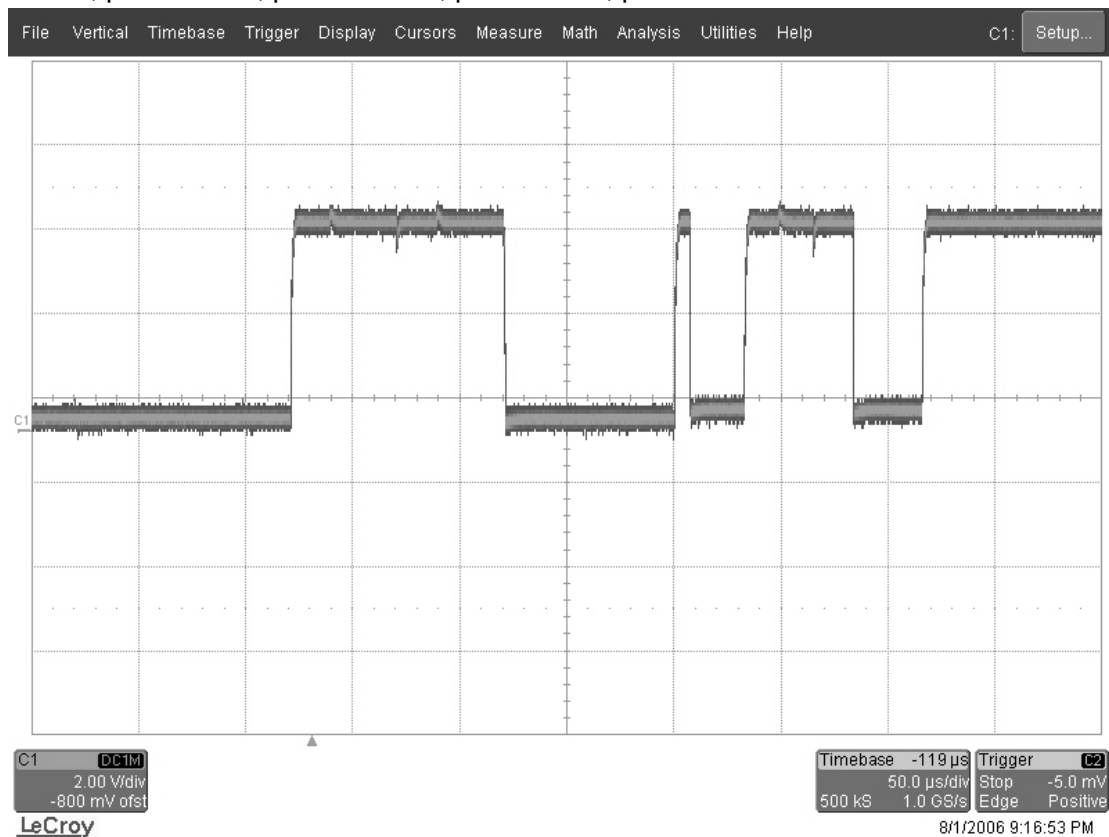
(1)RF inputting color bar signal, Composite Video Signal waveform at pin 14 of tuner U15, and the waveform at pin 169 of U1 (SVP-CX32LF) is like this:



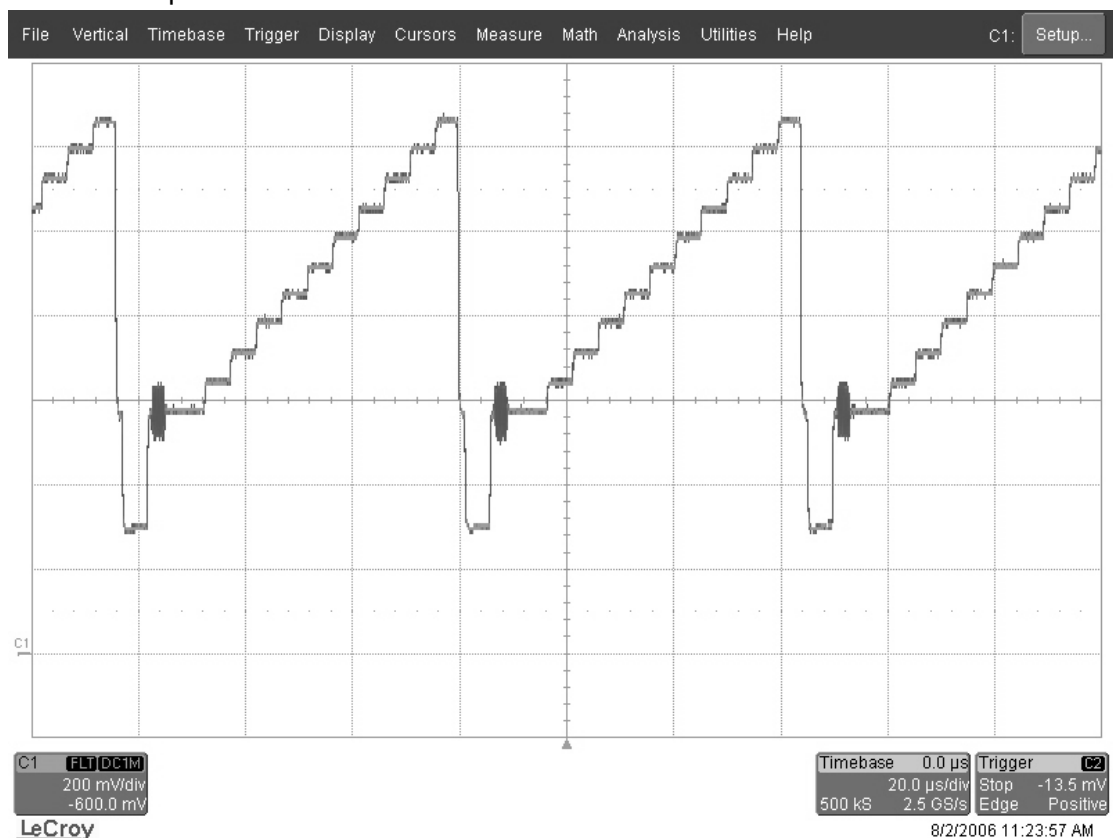
(2)RF inputting color bar signal, I²C bus clock signal SDA, pin 5, 6 of U31, pin 6 of U16, pin 39 of U35, pin 58 of U4, pin 40 of U30, pin 57 of U1, pin 4 of tuner U15:



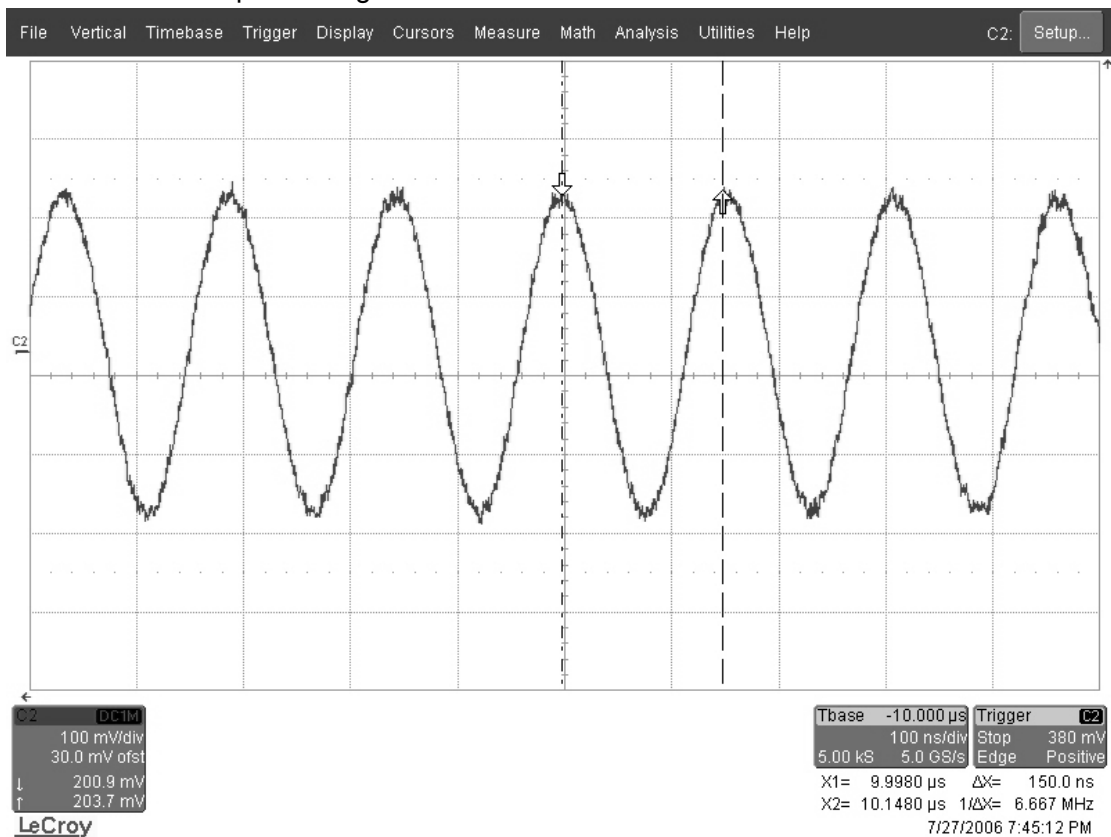
(3) RF inputting color bar signal, I²C bus clock signal SDA, pin 2, 3 of U31, pin 5 of U16, pin 40 of U35, pin 57 of U4, pin 39 of U30, pin 58 of U1, pin 5 of tuner U15:



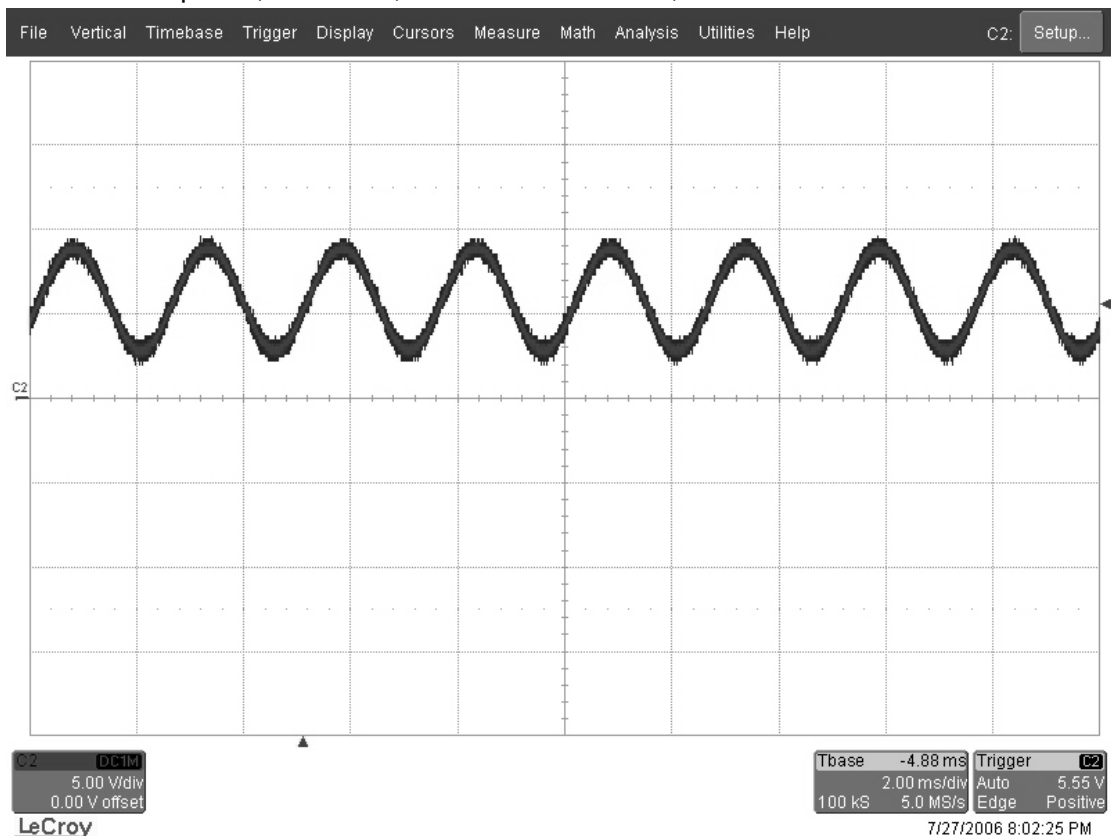
(4) RF inputting grey signal, Composite Video Signal waveform at pin 14 of tuner U15, and the waveform at pin 169 of U1 (SVP-CX32LF) is like this:



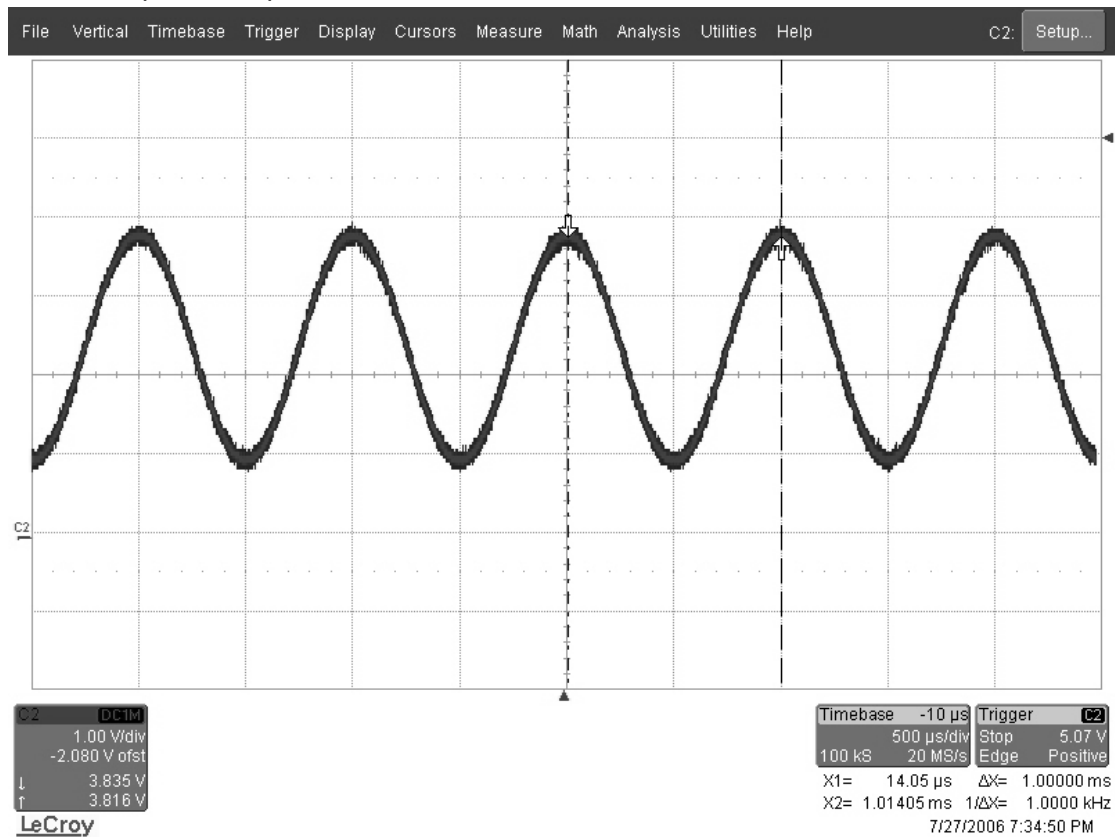
(5) RF inputting white signal, SIF Signal waveform at pin 11 of tuner U15, and waveform at pin 73 of sound effect processing IC Stv-8217:



(6) RF inputting white signal, and inputting sound signal with 1KHz frequency, inductance waveforms at pin 28, 29 of U35, and waveform of L26,L27:



(7) Inputting sound signal with 1KHz frequency, with the processing of U33 and power amplifier TDA8944J, waveform at pin 1, 4, 14, 17 of U33, and waveform at CON13 speaker and CON14 earphone output interfaces:



Chapter 4: Maintenance Procedure and Examples of Typical troubleshooting of problems

When you meet the following common problems, you might diagnose and get the solutions without contacting with the technicians.

Symptoms	Possible Reason	Solutions
No picture, no sound, and no indicator light on	1.The power cord is not plugged in 2.The power is off	1.Plug the power cord in 2.Turn the power on
Picture and sound with abnormality	1.Contrast, sharpness, and color are set improperly 2.Color system is set improperly 3.Sound system is set improperly	1.Adjust the value of Contrast, sharpness, and color 2.Set the Color system to the country broadcasting standard 3.Set the Sound system to the country broadcasting standard
Picture is spotted or with snow	Signal source is low-grade or the signal cord is in a lower quality	Use the qualified signal cord
No picture, no sound and indicator light is green	Contrast, brightness, color and volume are all in the minimum value or TV is in mute mode.	Adjust the value of contrast, brightness, color and volume
	The signal cable is not correctly connected.	Connect the signal cable correctly
Blue screen, AV or SVIDEO is displayed	There is no signal input or the video cable is not connected or incorrectly connected	Connect the video cable correctly
Picture is unclear or shaking or with black horizontal strips (in VGA mode)	VGA picture is not correctly adjusted.	Enter into "SETUP" menu, select "Auto Tracking" item to perform automatic calibration and adjust "Phase" to solve the problem
VGA picture is not centered		
No sound	There is no audio signal input or audio cable is not connected correctly	Connect the audio cable correctly
VGA picture display with improper color	The color temp is adjusted incorrectly by user	Readjust the color temp, or select the original color setting
HDMI source, with snow pixel of full screen	The source generate is not standard	Plug the HDMI cable again
The remote control does not work	Batteries are improperly installed or exhausted	1.Make sure the positive and the negative polarities are correct. 2.Check if there is a loose contact between the batteries and the springs 3.Replace the batteries

Chapter 5: Spare Part List

This listing of maintenance and repair parts are presented for reference only, modification of parameters will not be informed. For accurate models or specifications, please consult the newest data of our company. (LT32GJ01E is taking an example)

Number	Name	Part number	Print plate number	Proportion of easy damage (%)
1.	Panel frame	JUG6.116.623		0.1
2.	Back cover	JUG6.116.624		0.1
3.	Mount part	JUJ7.356.005		0.1
4.	Mainboard part	JUG6.690.106	Print plate JUG7.820.126	1
5.	Remote receiving board part	JUG6.695.028	Print plate JUG7.820.016	0.5
6.	Keyboard part	JUG6.694.029	Print plate JUG7.820.017	0.5
7.	Inner power module	JSK4210-014	Inner power module	5
8.	LCD screen	V320B1-LXX	LCD screen	0.1
9.	Electronic tuner	JS-6G1/111A25-A 2	Electronic tuner	0.5
10.	Electronic tuner	JS-6G2/121A25-A 2	Electronic tuner	0.5
11.	Dynamic speaker	YDT613-A9-10W- 8Ω	Dynamic speaker	2
12.	Dynamic speaker	YDG52-A3-10W-8 Ω	Dynamic speaker	2
13.	Remote control emitter	GK23J3	Remote control emitter	1

Chapter 6: Factory Setup and notice

1. Enter factory menu

Switch on TV set, and make LCD at operating state:

- ① Press **【MUTE】** key on remote control;
- ② Press “MENU” key on remote control, and switch to “SOUND” option with **【V+】** , **【V-】** key;
- ③ Move cursor to “Balance” option with **【P+】** , **【P-】** key to enter setting status;
- ④ Press number key “3”、“1”、“3”、“8” on remote control to enter password.

Entering factory mode is finished. Press **【Power】** key to switch off the TV and to quit factory mode.

(1) Factory menu display is presented like bellow:

chassis: LS01

Jul 29 2006 23:25:16

Version: LSE01-M32-V1.05WL

I² C off

Clear E² PROM

Panel Control

Factory Setting

System Control

Min/Max CONTROL

White Balance

Hotel Option

E² PROM Edit

Register Edit

Notes: “chassis: LS01” is the model number of local module, “Jul 29 2006 23:25:16” is the latest upgrading time for software, and “Version: LSE01-M32-V1.05WL” is the version number of current software.

(2)The detailed setting items are given bellow:

Contents of first page:

Setting item	Setting content	Setting method	Remark
IIC Off	Stop I ² C bus communication	“OK” or “V+” , “V-” key	Used for updating program
Clear EEPROM	E ² PROM initialization	Press “OK”key first, then press “V-” key	Only done in first setting station
Panel Control	Screen back light brightness control(or select the panel type)	Press “V+” , “V-” keys to enter submenu	
Factory Setting	Factory Setting	Press “V+” , “V-” keys to enter submenu	
System Control	System Control	Press “V+” key to enter submenu	
Min/Max Control	Analog datum setting	Press “V+” key to enter	Only set sub

	of picture and sound	submenu	brightness Bri Mid
White Balance	White balance parameters setting	Press “V+” key to enter submenu	
Hotel Option	Hotel mode	Press “V+” key to enter submenu	Used for hotel TV
E ² PROM Edit	E ² PROM data editing	No setting	
Register Edit	Register	No setting	

Use 【P+】 and 【P-】 keys on remote control to make up or down option, and use 【V+】 and 【V-】 keys to set.

Contents of sub pages:

Panel Control

Setting item	Setting value	Remark
LVDS Mapping	0x09	Polarity of LVDS signal
Backlight	100	Back light brightness value 1
SavePower1	50	Back light brightness value 2
SavePower2	30	Back light brightness value 3
BL-invisible	Off	Show SavePower mode in menu or not (ON: not show; OFF: show)
Panel type	CMO	Choose the type of the LCD screen to get the right parameter

Factory Setting

Setting item	Setting value	Remark
Balance	-50_0_50	Fast check of the balance of L/R sound channel
Volume	0_10_20..._100	Fast setting of volume, each step is 10
IIS	On/Off	Preset sound decoding IC of HDMI
Def Country	Other	Default country
RTC En	On/Off	Show real time clock or not
CANAL-Visual	On/Off	Open Canal+ function to user or not
Tuner Select	XG	Choose the type of Tuner (Europe market only)
Factory Out	>>	Output the factory settings

System Control

Setting item	Setting value	Remark	Setting item	Setting value
Default Lang	English	Default OSD language	SSC	
L/L' AGC	5	L/L' sound AGC	Delta	0
Over Modulation	On/Off	Over Modulation switch	Positive	6
PreScI SCART	8	SCART L/R input amplitude prescale	Negative	6
PreScI AM (or PreScI Mono	12	AM_MONO IF prescale (Mono IF prescalar)	Write	

for America)				
PreScl FM (or PreScl stereo for America)	12	FM_MONO IF prescale (Stereo IF prescale)		
PreScl NICAM (or PreScl SAP for America)	19	NICAM sound IF prescale (SAP IF prescale)		
EQ-invisible	Off	Equalizer switch , “Off” is 5 section equalization, “On” is high/low pitch setting		
ATS	Off	Program auto sequencing switch		
Logo	Off	Starting blue background LOGO switch		
Logo Edit		LOGO display contents, “V+”、“V-” for choosing setting position,, “P+”、“P-” for choosing letter , including 52 English big/small letters together		
Logo Color	Logo color	Modified according to user’s require		

Min/Max Control

Setting item	Setting value	Setting item	Setting value
Con Min	30H	Vol Min	00H
Con Mid	70H	Vol Mid 1	01H
Con Max	A2H	Vol Mid 2	14H
Bri Min	00H	Vol Mid 3	28H
Bri Mid	8DH	Vol Mid 4	4BH
Bri Max	A0H	Vol Max	64H
Col Min	00H	Tre Min	00H
Col Mid	40H	Tre Mid	30H
Col Max	70H	Tre Max	60H
Tnt Min	20H	Bas Min	00H
Tnt Mid	80H	Bas Mid	30H
Tnt Max	E0H	Bas Max	60H
Shp Min	00H		
Shp Mid	60H		
Shp Max	A0H		

White Balance

Normal		Warm	
R Gain	7DH	R Gain	7DH
G Gain	80H	G Gain	80H
B Gain	9AH	B Gain	9AH
R Offset	80H	R Offset	84H
G Offset	80H	G Offset	80H
B Offset	74H	B Offset	74H

Cool			
R Gain	7DH		
G Gain	80H		
B Gain	9AH		
R Offset	80H		
G Offset	80H		
B Offset	90H		

Hotel Option

Setting item	Setting value	Remark
Hotel Mode Enable	No	Hotel mode presetting (Yes——users can enter into Hotel mode, No——users can't enter into Hotel mode)
Force Pos	00	No use

Notes:

A. In “Min/Max CONTROL” setting item, “Bri Mid” item is used to set sub brightness of picture;

B. White balance needs to be set in “Normal” mode;

C. Set CLEAR E² PROM will clear the memory data, So do not set it unless it is needed; other setting items do not need setting.

2. Setting method of factory menu

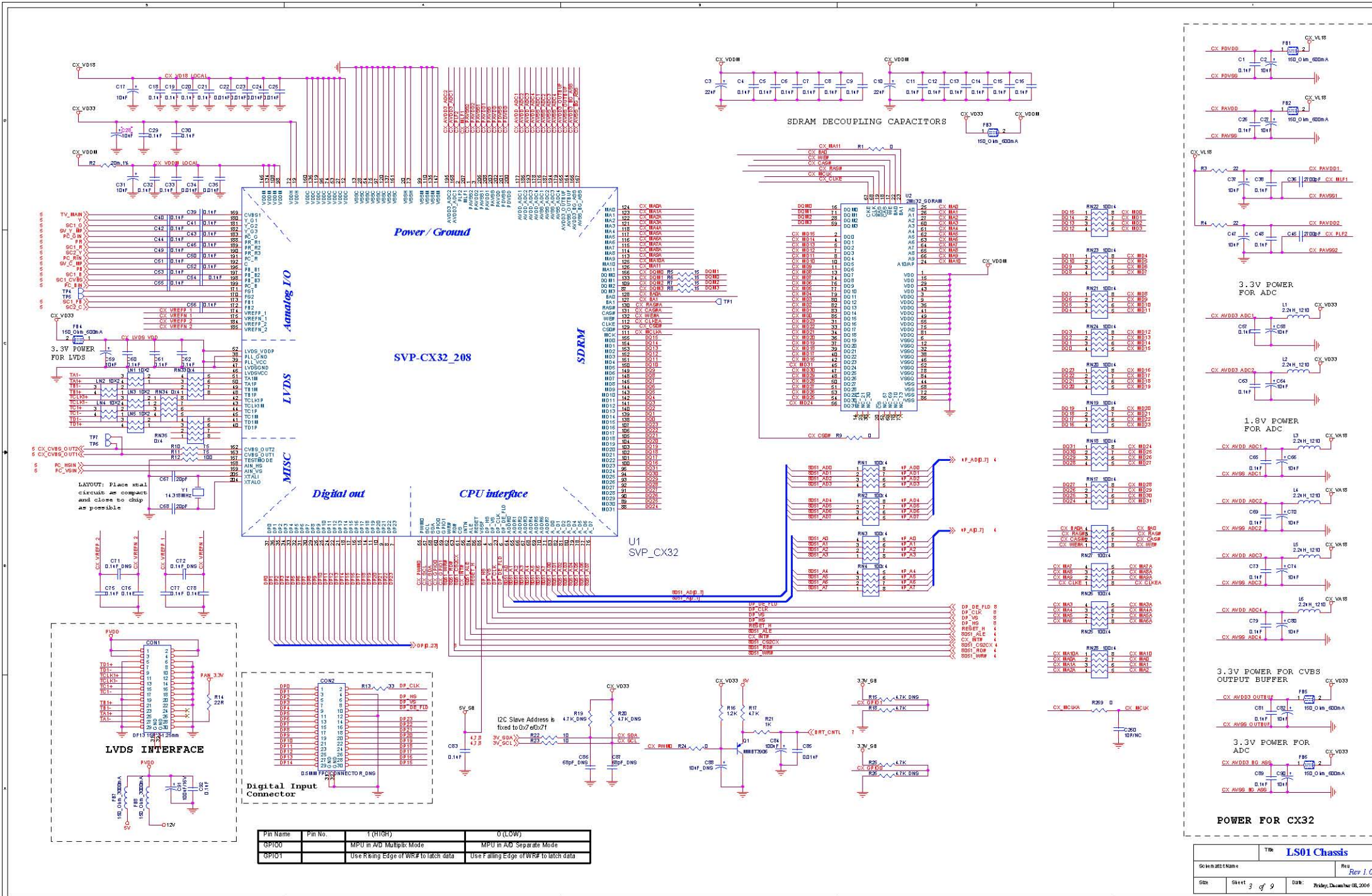
(1) Choose setting item

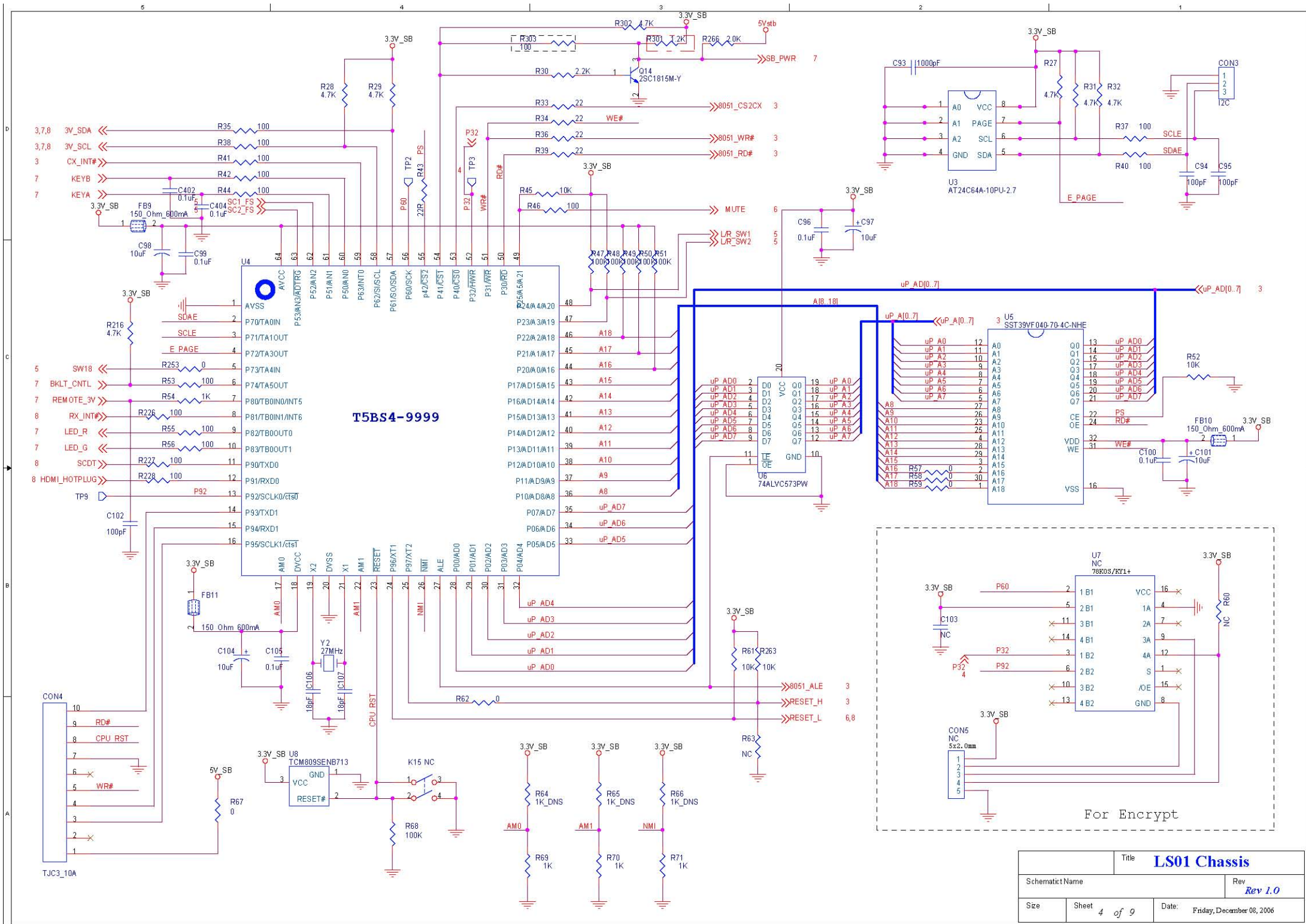
Operators can choose setting item orderly with【P+】and【P-】key, font having background display represents the item has been chosen. Press 【V+】 key to enter sub directory. Use 【P+】 and 【P-】 keys on remote control to make up or down option, and use 【V+】 and 【V-】 keys to set.

(2)All the menu functions are opened in factory mode, item checking and effect testing can be done by using menu if it is needed.

(3)Switching TV signal in factory mode can be done by directly pressing the number key. Press【MENU】key to back to the parent of working directory, press【DISPLAY】key to quit factory mode.

Appendix 1
LS01 module (taking LT32GJ01AUB for example) Circuit Schematic Diagram





[illegible]

Component2 And
CVBSout Socket
Only For Asia&USA
Market

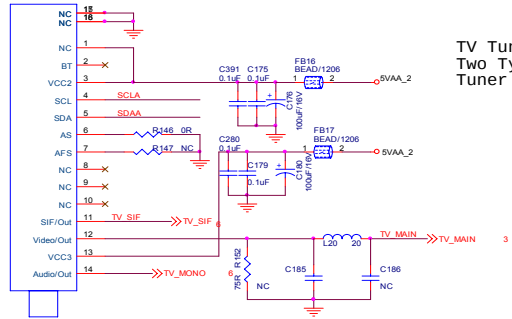
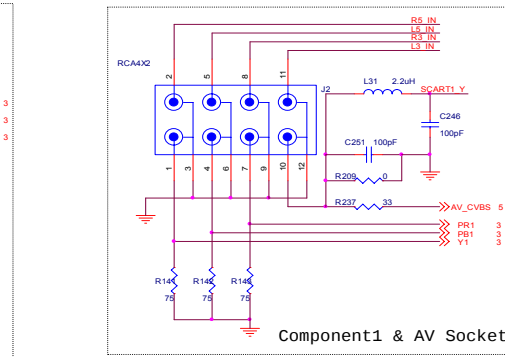
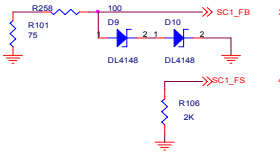
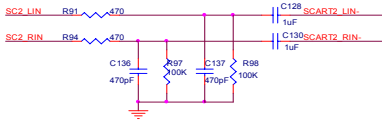
Component2 and CVBSout Socket Only For Asia/USA Market

The diagram illustrates the wiring for the CVBSout Socket (Component2) for the Asia/USA Market. It features an RCA42 connector (J1) with pins 1 through 11. The connections are as follows:

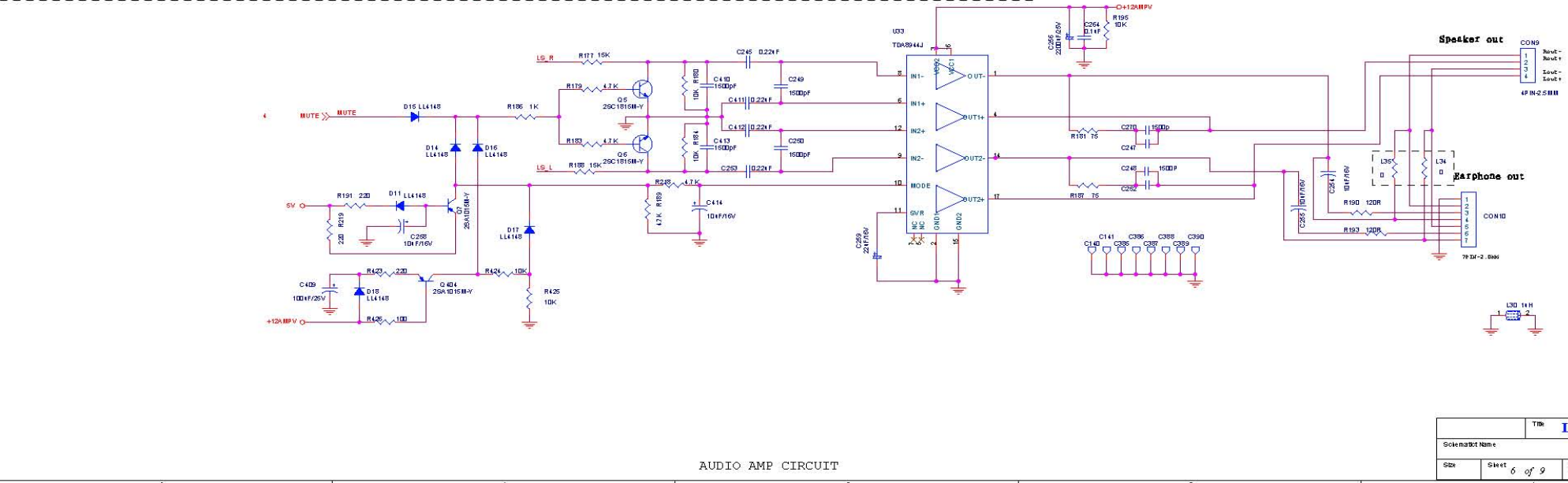
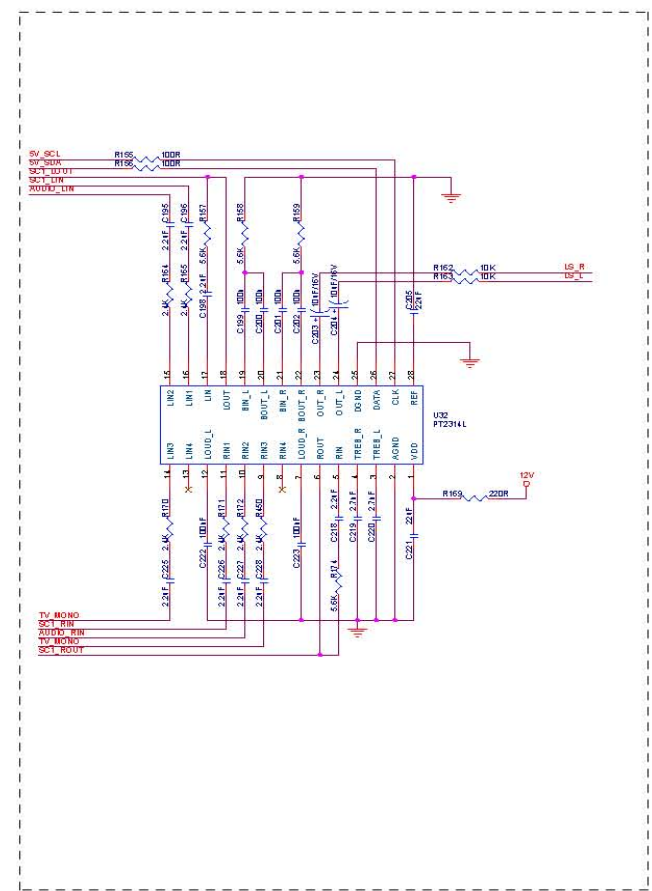
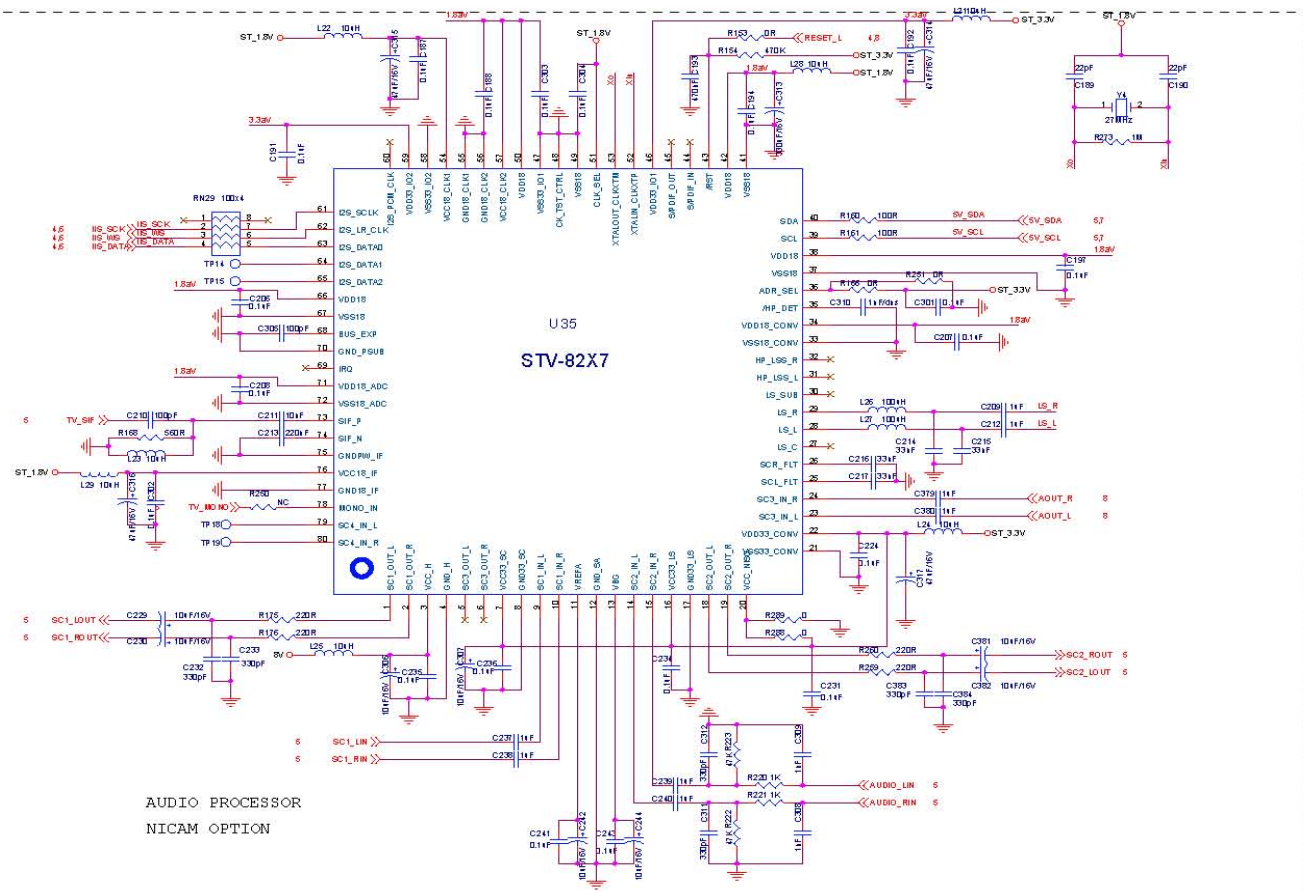
- Pin 1: DVB-Y4
- Pin 2: DVB-Pb4
- Pin 3: DVB-Pb4
- Pin 4: DVB-Pb4
- Pin 5: DVB-Pb4
- Pin 6: DVB-Pb4
- Pin 7: DVB-Pb4
- Pin 8: DVB-Pb4
- Pin 9: DVB-Pb4
- Pin 10: DVB-Pb4
- Pin 11: DVB-Pb4

Additional connections include:

- SC2_LIN: Connected to pin 10 via resistor R219.
- SC2_RIN: Connected to pin 11 via resistor R277.
- SC1_ROUT6: Connected to pin 11 via resistor R282.
- DVB-L4: Connected to pin 11 via resistor R278.
- DVB-R4: Connected to pin 11 via resistor R280.

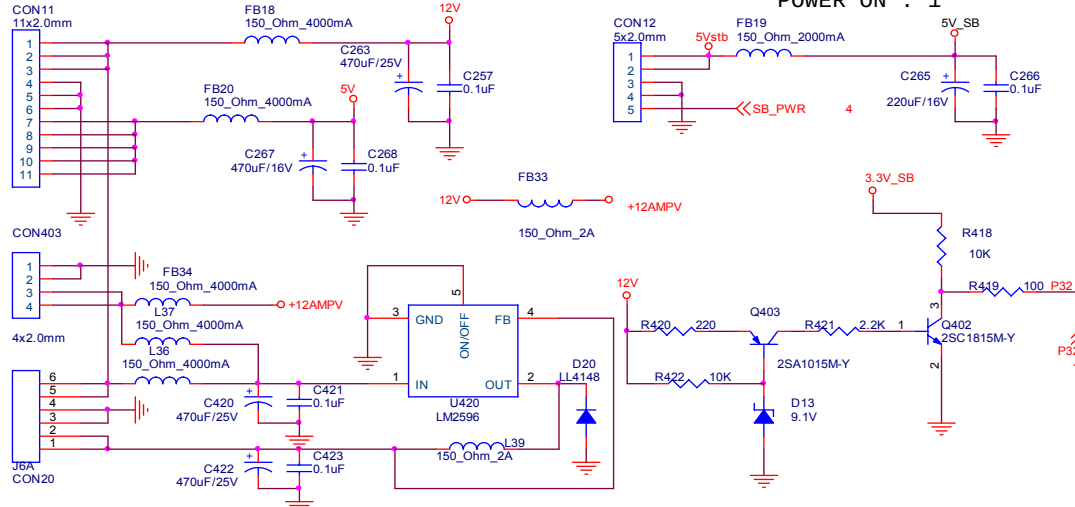


		Title LS01 Chassis	
Schematic Name			Rev Rev 1.0
Size	Sheet 5 of 9	Date: Tuesday, April 24, 2007	

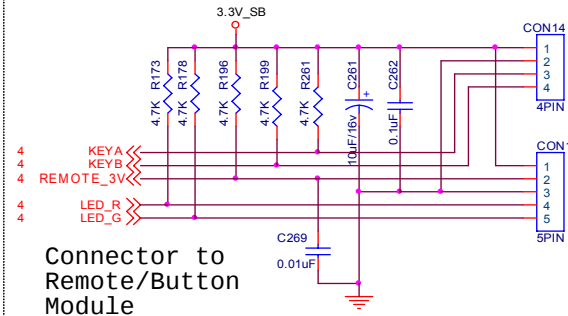


POWER SUPPLY INPUT INTERFACE POWER SUPPLY MODUEL USE MEGMEET MLT186

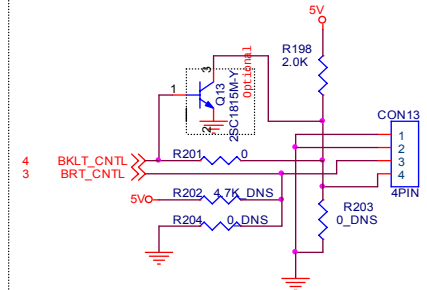
STANDBY : 0
POWER ON : 1



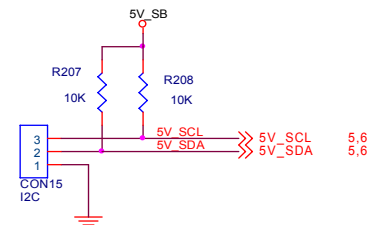
Connector to Remote/Button Module



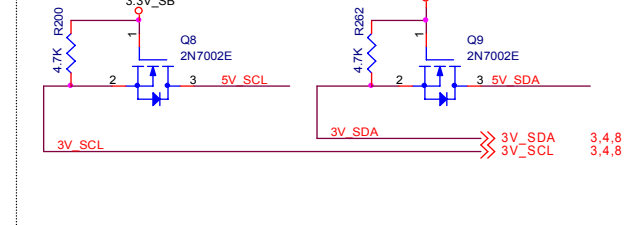
BACKLIGHT CONNECTOR



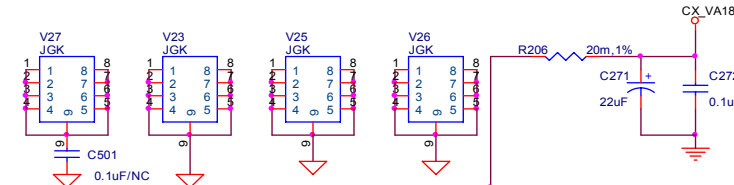
I2C TOOL DEBUG INTERFCE



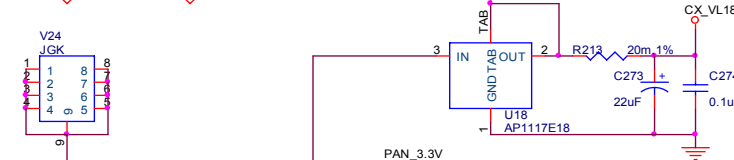
I2C DATA LEVEL CHANGE CIRCUIT



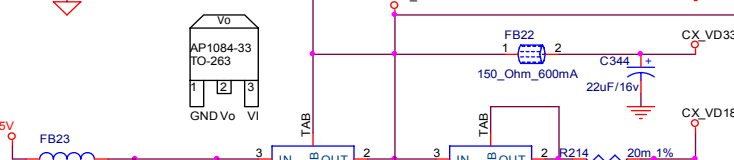
SVP-CX32 1.8V Analog Power



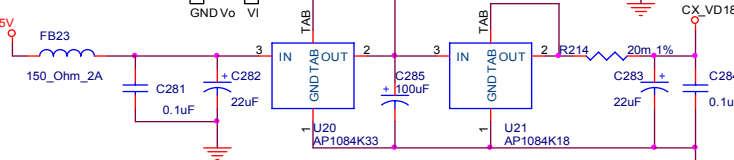
SVP-CX32 1.8V PLL Power



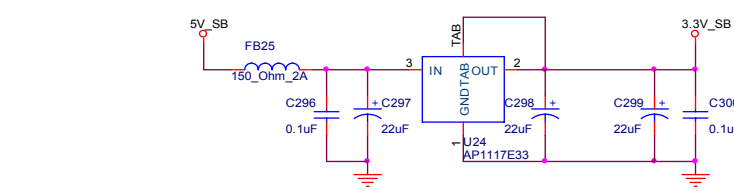
SVP-CX32 3.3V Digital Power



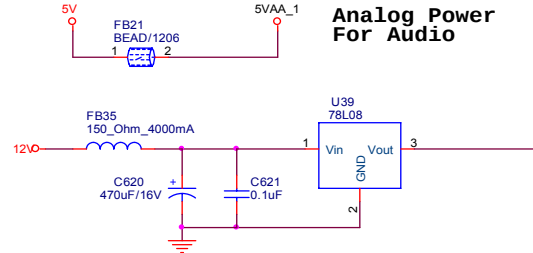
SVP-CX32 1.8V Core Power



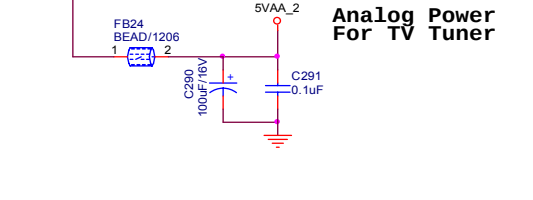
3.3V Stand By Power



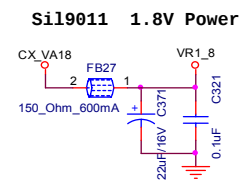
Analog Power For Audio



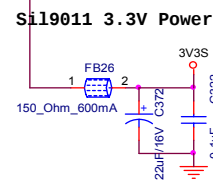
Analog Power For TV Tuner



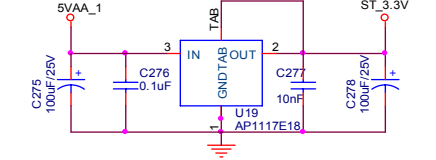
Sil9011 1.8V Power



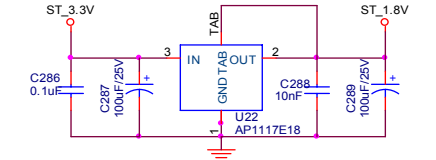
Sil9011 3.3V Power



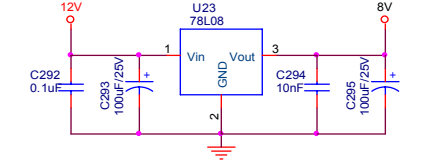
ST82X7 3.3V Power



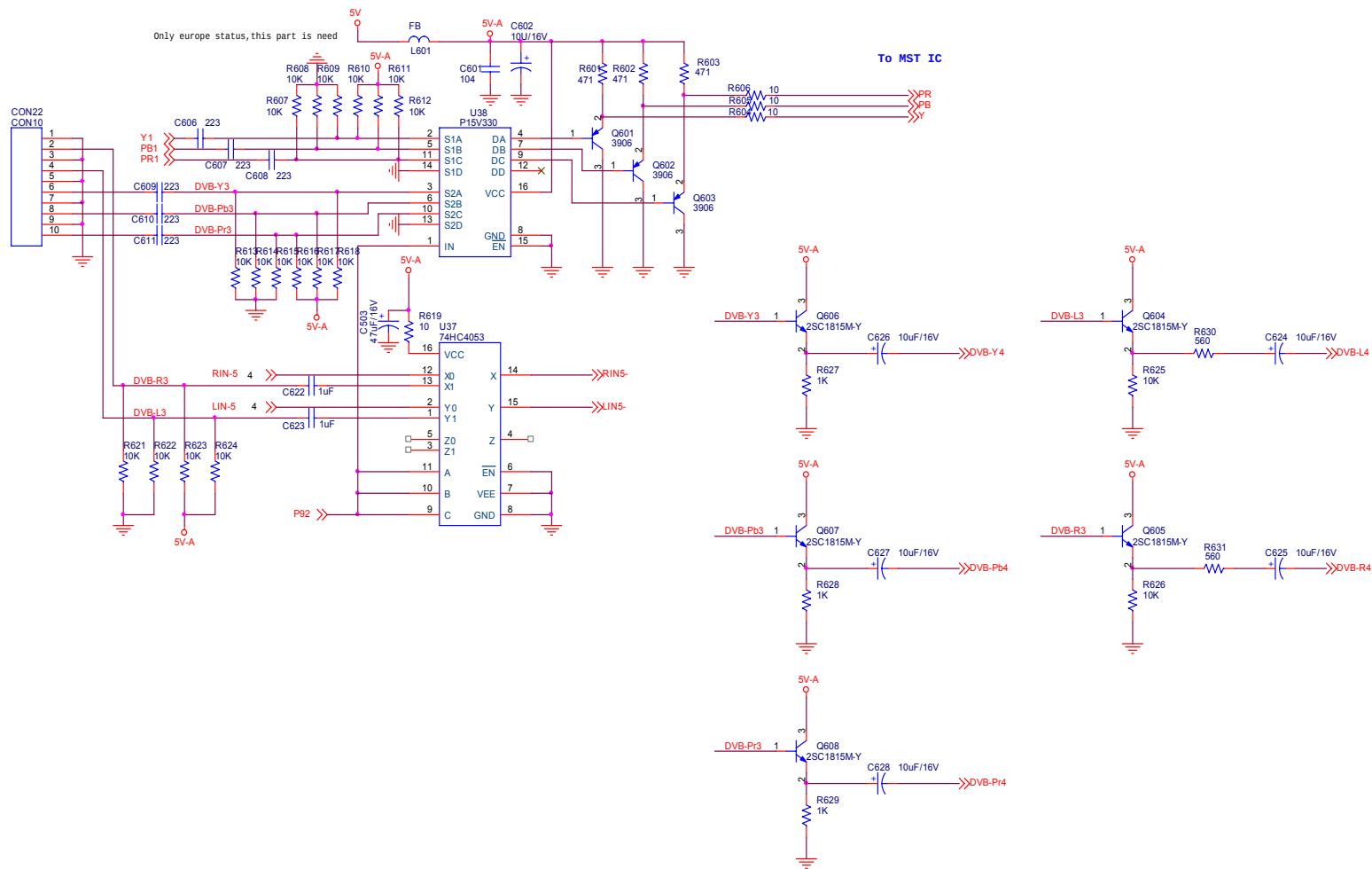
ST82X7 1.8V Power



ST82X7 8V Power

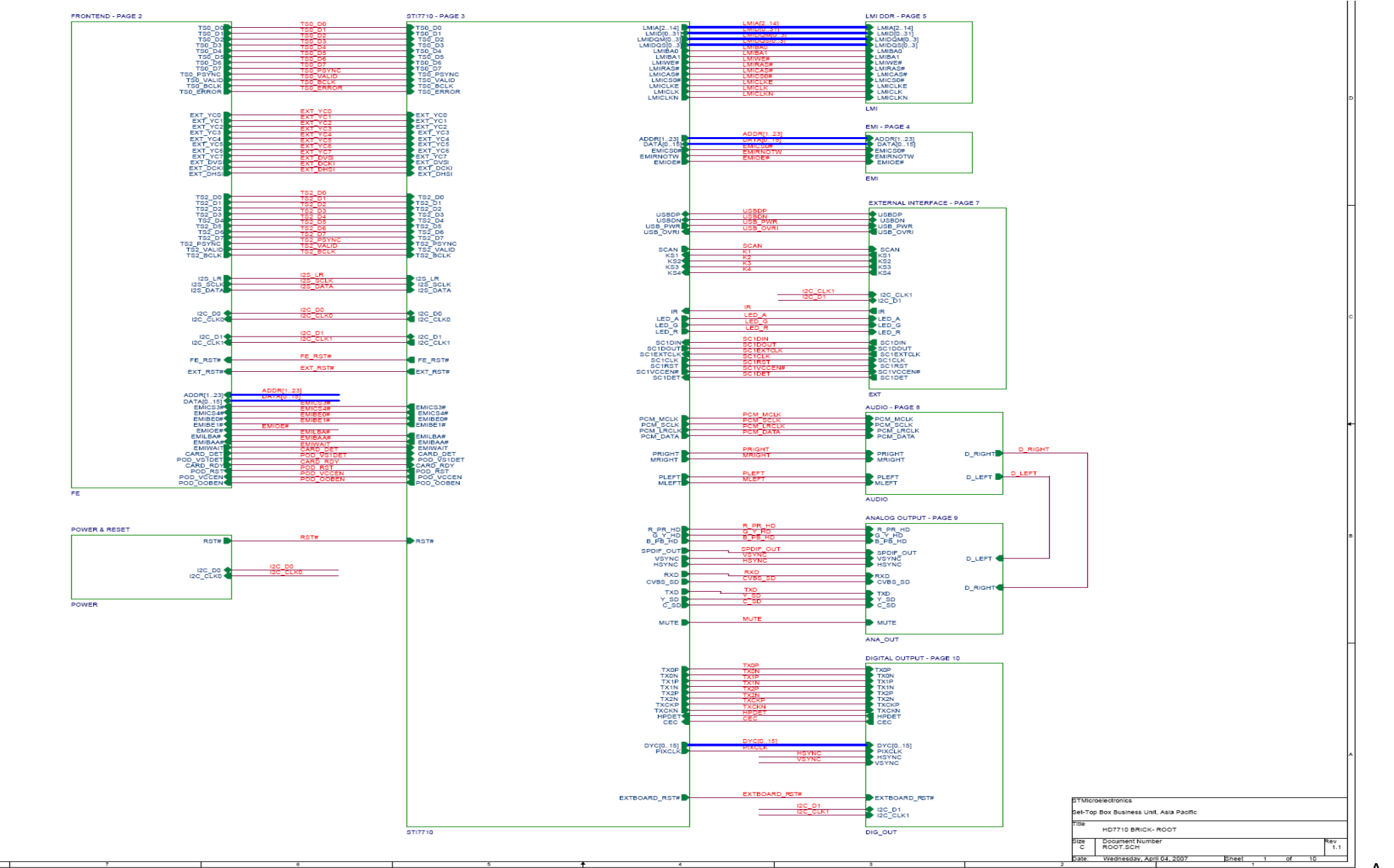


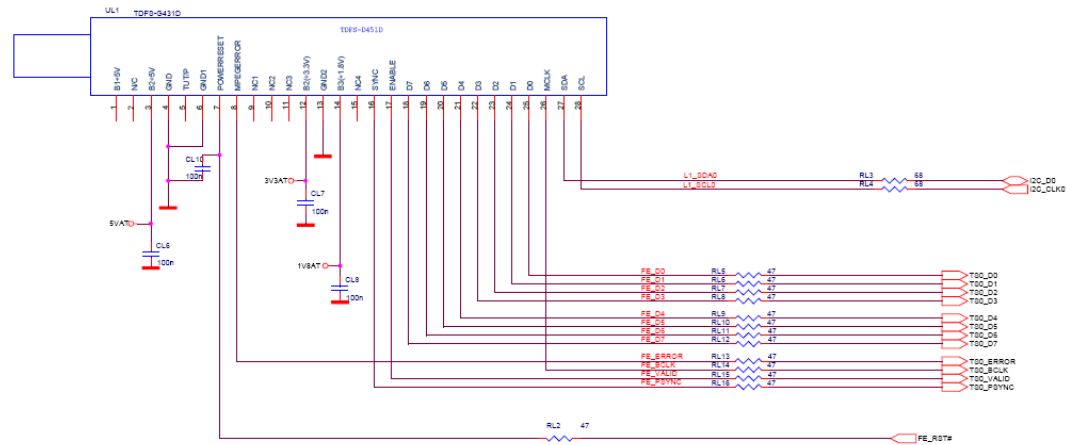
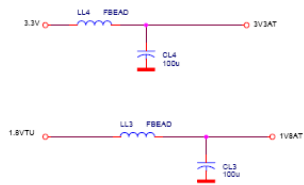
Title		
LS01 Chassis		
Schematic Name		Rev 1.0
Size	Sheet 7 of 9	Date: Wednesday, April 25, 2007



		Title LS01 Chassis	
Schematic Name			Rev Rev 1.0
Size	Sheet 9 of 9	Date: Thursday, April 26, 2007	

Appendix2-DVB-T module:

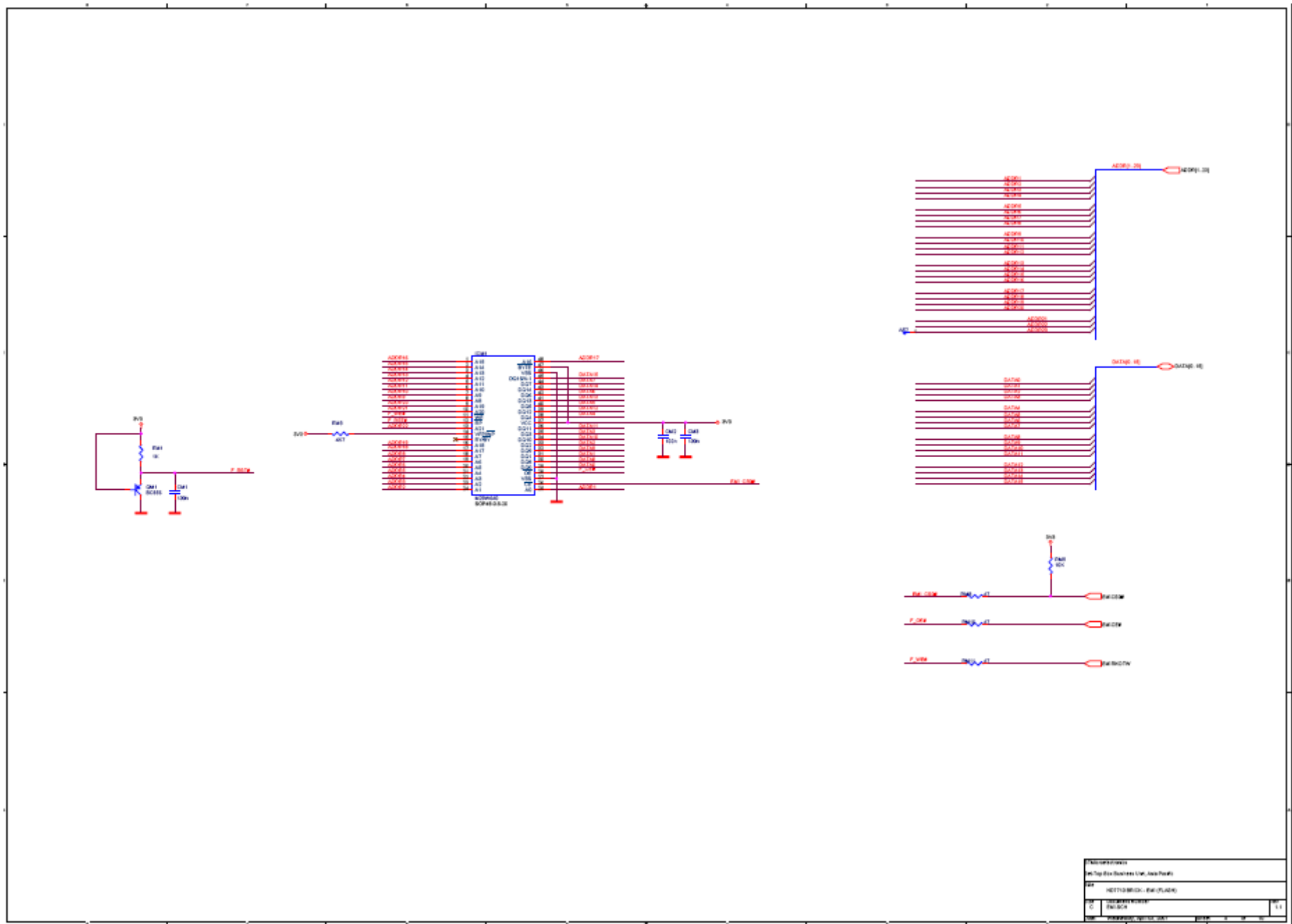




EXTERNAL TRANSPORT STREAM INPUT 0

EXTERNAL CABLE CARD INTERFACE

STMicroelectronics			
Del-Top Box Business Unit, Asia Pacific			
File			
HD7710 BRICK - ST-NIM AND EXTERNAL FE			
Size			
C	Document Number	FE-804	Rev
0	FE-804		1.1
Date: Wednesday, April 25, 2007 Sheet 2 of 13			





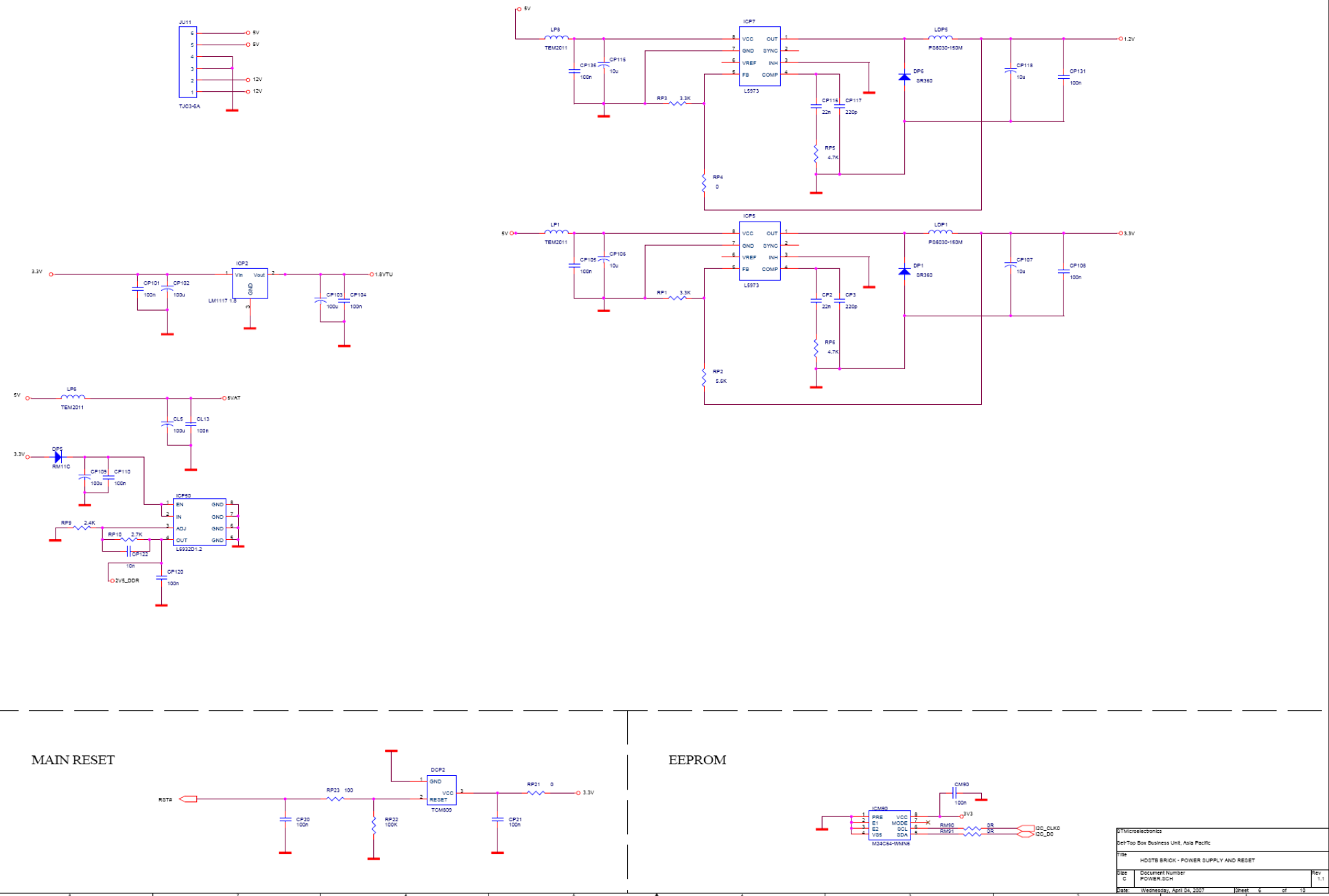
Get Top 500 Ranking on Yelp, Angie's List

HOTTENBACH, LAW DON

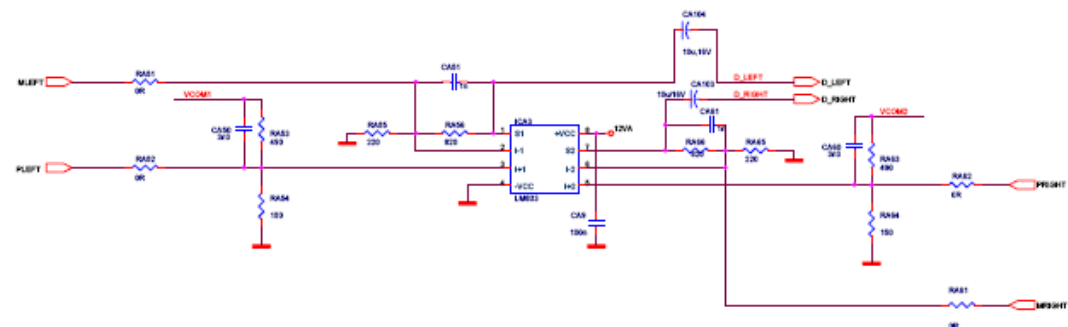
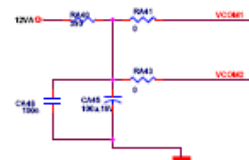
FORM	CONTRACTING METHOD
C	L&B-BCH

NAME	DATE

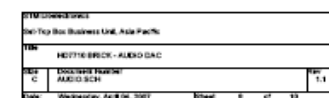
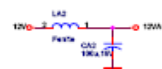
POWER SUPPLY INTERFACE



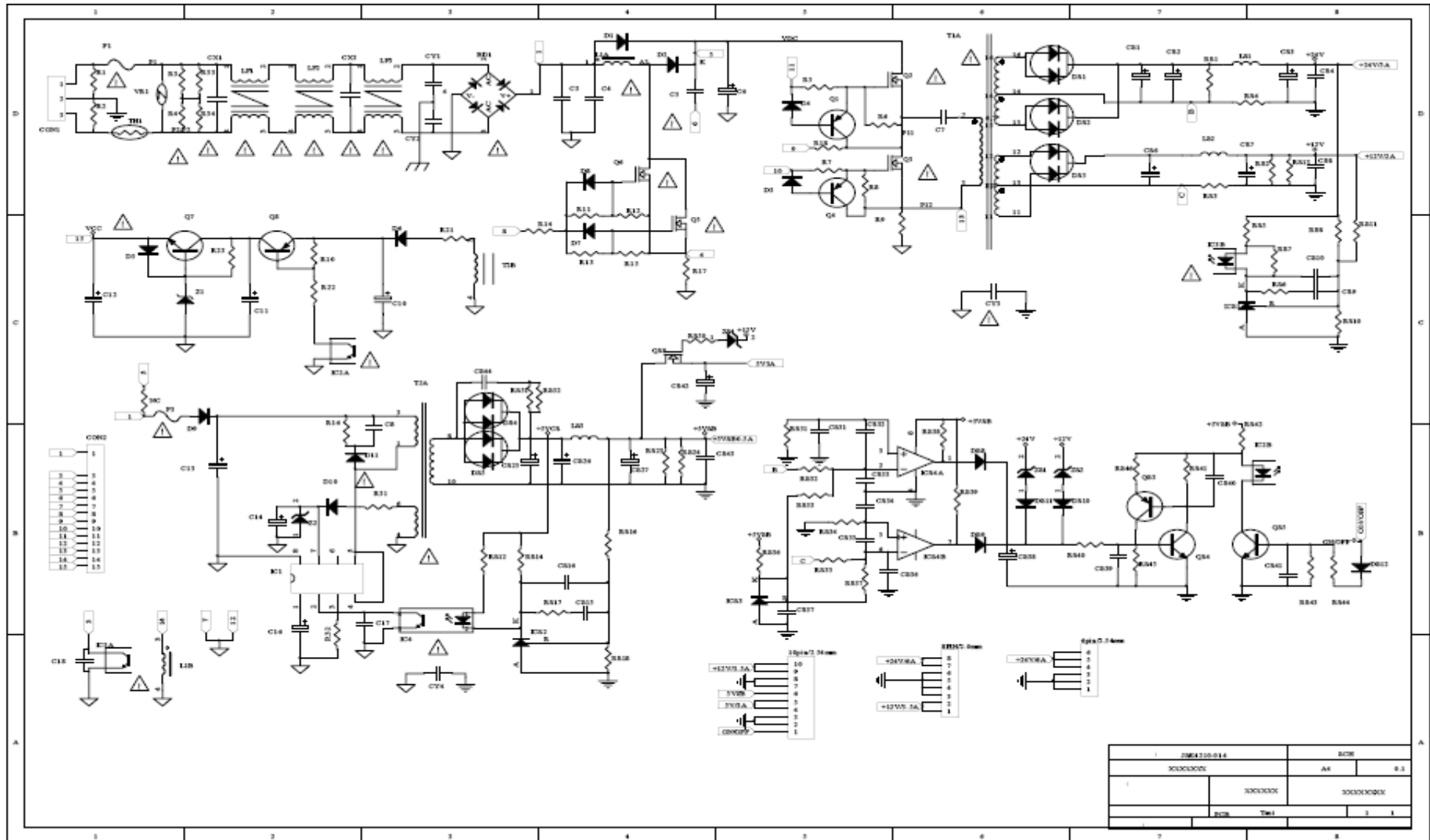
BTMicroelectronics	
Del-Tap Box Business Unit, Asia Pacific	
File: H05TB BRICK - POWER SUPPLY AND RESET	
Size: C	Document Number: POWER.SCH
Rev: 1.1	
Date: Wednesday, April 25, 2007	
Sheet: 6 of 18	



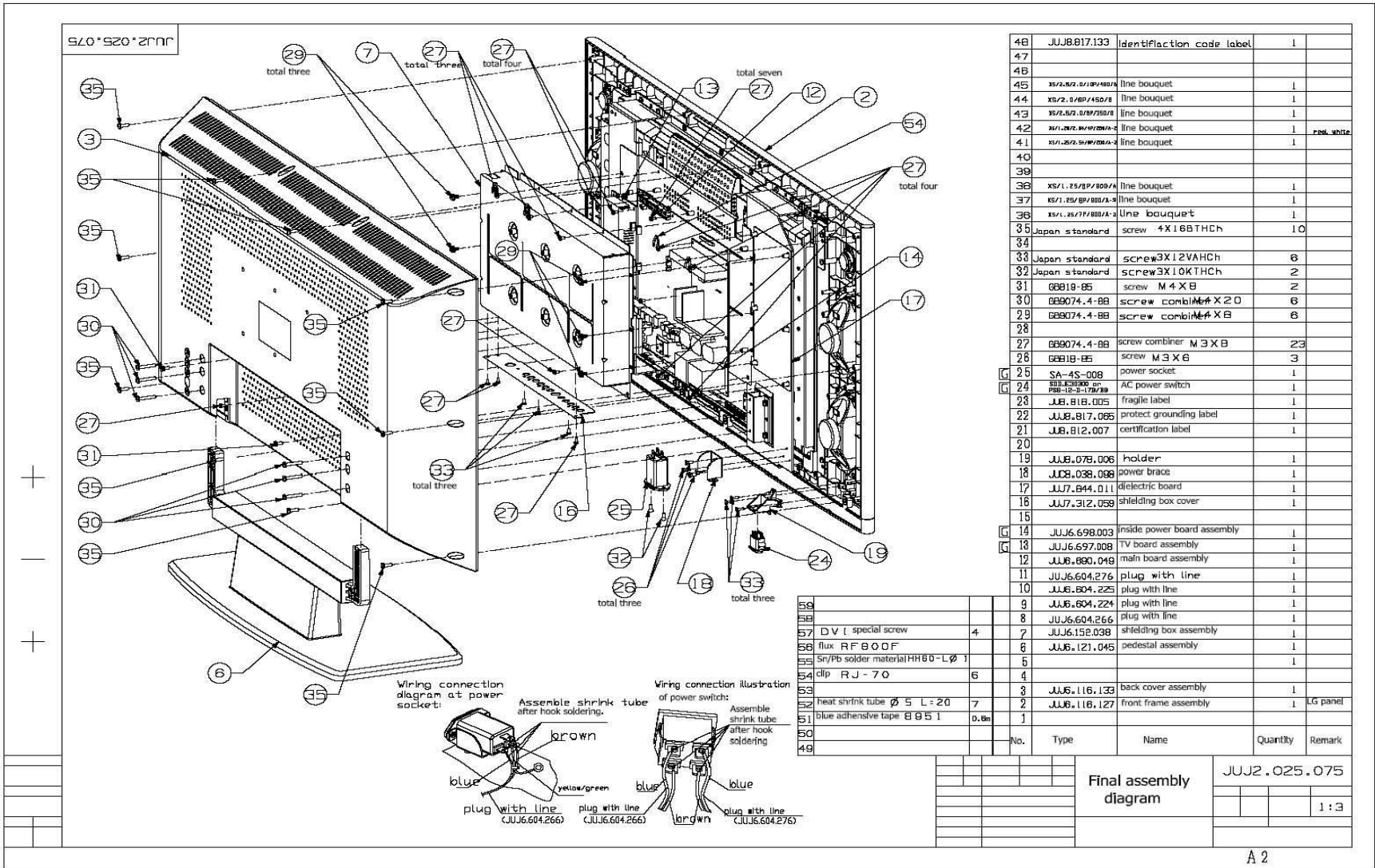
STM32F405			
STM32F405			
HEXTECH - AUDIO DAC			
REV	1.0	1.0	1.0
IC	STM32F405	1.0	1.0
Rev	1.0	1.0	1.0

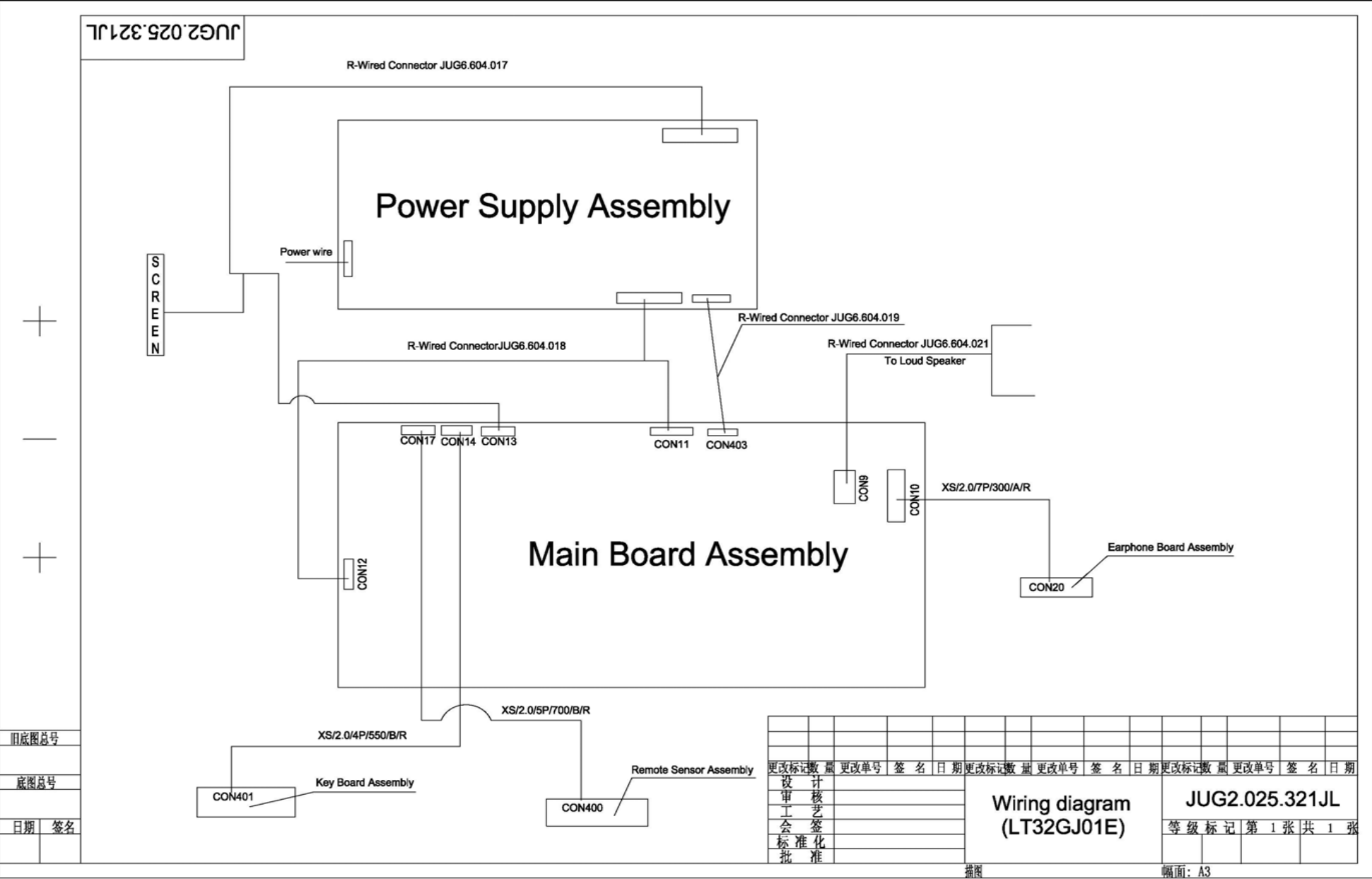


Appendix 3 Power Module Schematic Diagram



Final Assembly Diagram LT2618





旧底图总号	
底图总号	
日期	签名